Application Note

Akademie věd České republiky
Ústav teorie informace a automatizace AV ČR, v.v.i.

UTIA EdkDSP Demonstrator in Xilinx 3S700AN FPGA with Embedded FLASH and NV RAM

Jiří Kadlec
kadlec@utia.cas.cz
phone: +420 2 6605 2216
UTIA AV CR, v.v.i.

Revision history:

Rev.	Date	Author	Description
1	27.12.2012	Jiří Kadlec	Doc. text completed.
2	31.12.2014	Jiří Kadlec	Ready for publication on UTIA www.
3	3.1.2015	Jiří Kadlec	Update of photos

Acknowledgements:

This work has been partially supported by the ENIAC JU project “Pilot line for advanced nonvolatile memory technologies for automotive microcontrollers, high security applications and general electronics” (PANACHE). PANACHE is an **ENIAC JU** project no. ENIAC JU 621217. This work has been also partially supported by the Ministry of Education Youth and Sports of the Czech Republic project No. 7H14006. This project is providing the Czech Republic part of funding for the ENIAC JU project PANACHE.

Table of contents

1. Summary

1.1 Key features

This application note describes designs for Xilinx Spartan3AN FPGA 3S700AN [1] with serial configuration FLASH embedded in the FPGA chip [5]. The note describes use of an UTIA EdkDSP demonstrator package [9]. The document explains how to install and use the demonstrator on Windows7, (32 or 64 bit). Package [9] can be also installed and used without modification on x86 PC with Linux PC or Windows XP (32 or 64 bit).

The package [9] includes demo SoC systems based on Xilinx, area-optimized, MicroBlaze processor [11] and 0 up to 3 I/O subsystems based on PicoBlaze processors [10]. These controllers serve for processing of I/O operations and work with fixed firmware. These PicoBlaze processors are interfaced to another PicoBlaze processor. It serves for scheduling of vector floating point operations in the UTIA EdkDSP configurable floating point data path. This PicoBlaze is programmable from the MicroBlaze application programs in the runtime. The MicroBlaze processor is executing application software from an external 64 MB DDR2. This application SW and the EdkDSP firmware programs are initially loaded by the first-stage boot-loader from an external, 4 MB parallel NOR Flash. The EdkDSP firmware programs and data can be downloaded/uploaded to/from the DDR2 based file system via 10/100 Mb Ethernet p2p connection served by TFTP server running on MicroBlaze. XGA 1024x768p70 video display is supported. WWW internet explorer user GUI is supported by HTTP server running on the MicroBlaze.

1.2 Use of designs in PANACHE project

Designs described un this app note serve as examples of relatively low cost system serving as low power IoT device. The targeted applications have to have low requirements on the Ethernet data exchange, but relatively high requirements on security of the design against cloning. The configuration bitstream content and the initial firmware programs can be protected by the automatic configuration from the eFLASH present in the chip. After the power-up, the programmable logic of the 90 nm 3S700AN device is configured by bitstream data. It is read internally from the 8 Mb serial eFLASH. The 32bit MicroBlaze processor and the three 8b PicoBlaze I/O controllers have the initial program firmware in internal RAM blocks. Data content of these RAM blocks is internally configured from data present in the bitstream. These automatically initiated program memory blocks will be called the non-volatile RAM or shortly NV RAM in this application note.

Main focus of the ENIAC JU project PANACHE [8] is the development and experimental pilot-line production of eFLASH devices embedded in the SoC integrated circuits designed in technologies 55nm, 40nm and possibly 28nm. UTIA is contributing to this project by design and development of demonstrators and SW application projects for these integrated circuits with internal eFLASH. Applications and designs presented in this application note have been developed by UTIA in the first year of the Eniac JU project PANACHE [8] for the already mature 90nm 3S700AN device [6]. These 3S700AN applications will serve as one of inputs for the comparison with other SoC IC devices developed in next 3 years (2015-2017) within the PANACHE project. Main parameters to be compared are:

- Operating temperature range (for the Commercial and for the Industrial grades).
- Performance in concrete application scenarios and user acceptance of this performance.
- Program cycles and data retention parameters of the internal eFLASH.
- Power consumption of the IC with internal eFLASH.
- Power consumption of the complete PCB system, with the complete power DC2DC regulators.
- Time to configure the HW after the power-up. From eFLASH to logic to NV RAM and start execution.
- Time to boot the application from the external NOR Flash to the external DDR2 and start execution.
- Presence of security features for protecting of the digital design and the initial firmware programs.
- The unit cost and the volume cost of the IC with the internal eFLASH and NV RAM blocks.

1.3 Summary of 3S700AN parameters.

This is summary of basic parameters of the 3S700AN device with the internal eFLASH:

Device (Xilinx)	**XC3S700AN (**XC3S700AN-4FGG484C)
System Gates	700 K
Equivalent Logic Cells	13,248
CLBs	1,472
Slices	5,888
Distributed RAM Bits	92 Kb
Block RAM 18Kbit blocks (potentially NV RAMs)	20
Block RAM Bits	360 Kb
Dedicated multipliers (18x18bit)	20
DCMs	8
Maximum user I/O	372
Max differential I/O Pairs	165
Bitstream size	2,669 Kb
FPGA technology	90 nm
eFLASH parameters	
In-System Flash Bits	8 Mb
Page size	264 bytes
Page size in an optional power-of-2 mode	256 bytes
Pages	4,096
Blocks	512
Sectors	16
In-System Flash technology	130 nm (X-FAB) and 110 nm (UMC) from 2014
Temperature range	
Commercial grade Temperature Range (TJ)	0°C to 85°C
Industrial grade Temperature Range (TJ)	-40°C to 100°C
eFLASH program cycles and data retention	
Program/Erase cycles	100,000
Data retention	20-year
Access modes	random accessible, byte addressable
Serial data transfers	up to 66 MHz
eFLASH data protection and security	
Sector protect	write- and erase-protect a sector (changeable)
Sector lockdown	sector data is unchangeable (permanent)
Security register	128 byte
eFLASH unique identification of each device	
Identifier unique to the in-system Flash	64 byte factory-programmed
User-programmable field	64 byte one-time programmable

Cost (Source: WWW of distributors, 30.12.2014)	
Cost USD (Digikey) XC3S700AN-4FGG484C	1: $41,16
Cost USD (Digikey) XC3S700AN-4FGG484I	1: $47,35
Cost GBP (Farnell) XC3S700AN-4FGG484C	1: £35.43 10: £30.46 100: £29.27 200: £28.7 300: £28.14
Cost USD (Avnet) 3S700AN starter kit [6]	1: $199,00 (HW-SPAR3AN-SK-UNI-G)

See [1], [2], [3], [4] and [5] for additional details.

1.4 Designs features

The designs described in this application note provide concrete measurable reference data for these features:

- The automatic internal configuration of the programmable logic and of the NV RAMs from the on-chip eFLASH significantly improves security. The content of NV RAM is not directly accessible.
- The PicoBlaze controllers [10] with fixed program firmware in the NV RAMs act as finite state machines dedicated to processing of the digital I/O. The concrete fixed PicoBlaze firmware is executed from the NV RAMs by PicoBlaze controllers with the performance compatible to other parts of the design (75 MHz clock).
- All designs described in this app note support low-speed 10/100 Mb Ethernet connectivity.
- All designs support the XGA RGB565 video display with the resolution 1024x768p70 with final output resolution reduced to RGB444 by simple resistor based D/A.
- Some designs implement an adaptive acoustic noise cancellation. Demonstrated accelerators compute the recursive adaptive LMS algorithm for regression filter with 250 coefficients with the sampling frequency 40 KHz in single precision floating point arithmetic. This corresponds to the sustained performance of 40 MFLOP/s on 3S700AN device.
- The floating point 250 tap coefficients FIR filter (acoustics room model) is computed with the floating point performance 92 MFLOP/s on the EdkDSP accelerator. The peak performance of the EdkDSP accelerator (only theoretical) is 150 MFLOP/s on 3S700AN device.
- The EdkDSP accelerator is internally organised with single reconfigurable floating point data path.
- The floating point applications are scheduled inside of the EdkDSP accelerator by the Xilinx PicoBlaze processor. Each firmware program has maximal size of 1024 (18 bit wide words) and it is reprogrammable from the MicroBlaze in the runtime.
- The EdkDSP accelerator can be reprogrammed by change of the firmware. The programming is possible in C and ASM with the use of the UTIA EDKDSP C compiler. The accelerator can be programmed with two firmware programs. The application can swap the execution of the program in only few clock cycles in the runtime.
- The alternative firmware can be downloaded to the EdkDSP accelerator in parallel with the execution of the current firmware. This is demonstrated by swap of the firmware for the FIR filter room response to the firmware for the adaptive LMS identification of the filter coefficients in the acoustic noise cancellation demos.
- The EdkDSP floating point accelerator is (in case of the 250 tap adaptive LMS filter) 2200x faster than the area optimized, 50 MHz, MicroBlaze processor implementation. To save the area the MicroBlaze processor has no HW floating point unit, no HW fixed point multiplication support and only minimal 256B Instruction and Data caches. This area optimised PicoBlaze is still capable to run SW stacks with the LwIP libraries [7], needed for implementation of low performance Ethernet TFTP server, HTTP server and low-performance rendering of the NPI based XGA video output. The SW stack is running on top pf the Xilinx Xilkernel which is supporting the real time tasks and the Posix compatible pthreads.

1.5 What is included in this demonstrator

This 3S700AN evaluation package includes these deliverables for the Windows 7 (32 or 64bit) with the possibility (not documented in detail here) to be installed and tested also on Linux or Win XP (32 or 64bit):

- 12 evaluation versions of designs for the starter Kit 3S700AN [6]. All designs include one EdkDSP accelerator with single reconfigurable floating point data path. MicroBlaze works with 50 MHz clock, EdkDSP accelerator and XGA display controller works with 75 MHz clock, DDR2 works with 100 MHz clocks.
- Designs have been developed in the Xilinx XPS 14.5 tool chain.
- All designs include the Xilinx xps_ethernet_lite 10/100Mb Ethernet controller.
- All 12 precompiled designs include XGA RGB565 1024x768p70 video controller based on the direct access to the external DDR2 memory by the native port interface (NPI) of the Xilinx multi-port memory controller (MPMC).
- Larger SW demos are using the Xilinx Xilkernel OS, the LwIP package [7] and the Xilinx memory file system package xilmfs.
- UTIA is providing source code for the demo applications and SW projects for the Xilinx SDK 14.5. These source code projects are linked with UTIA libraries libwal.a, libjpg.a, librgb.a and libmfsimage.a.
- The UTIA EdkDSPC C compiler is provided in form of executable binary applications for an Ubuntu Linux 32bit executable in Windows 7 (32 or 64 bit). Ubuntu can run in VMware Player in Windows 7.
- The user part of the demonstration firmware is provided in source C code and it is also provided as precompiled binary files to enable the initial evaluation of the EdkDSP reconfigurable accelerators without installation of the UTIA EdkDSPC C compiler.

Demonstrator packages:

- The evaluation versions of the UTIA EdkDSP accelerators compiled in the designs have HW limit of maximal number of performed vector operations after each HW rest or complete power-off of the 3S700AN device. The evaluation designs and this application note can be downloaded for free after the e-mail registration in UTIA www page [9]. See sections 4-6 of this application note for specification of deliverables for PANACHE project partners and the license details.

- A free evaluation version of the EdkDSP package for Spartan SK 3AN700, PLB bus is offered by UTIA to the PANACHE project partners [8] for zero cost. It provides the Xilinx XPS projects for 3AN700, with the evaluation versions of EdkDSP accelerators for the Spartan SK 3AN700 in form of netlisted PLB pcores. See sections 4-6 of this application note for specification of deliverables for PANACHE project partners and the license details.

- A release version of the EdkDSP package for Spartan SK 3AN700, PLB bus is also offered by UTIA commercially. It provides EdkDSP accelerators for the Spartan SK 3AN700 in form of netlisted PLB pcores with the main HW limitation of the free evaluation packages removed. See sections 4-6 of this application note for specification of deliverables and license details.

2. Demonstrator of EdkDSP platform on 3S700AN board

2.1 Description of EdkDSP accelerators and evaluation designs

This application note describes how to set-up and use collection of 8 HW designs on Xilinx 3S700AN board [6] with PLB bus. The demonstrator serves to evaluation of parameters of these floating point accelerator families:

- **bce_fp11_1x1_0_plbw_v1_[1x|2x|3x]_a** is a family of four floating point accelerators with single reconfiguravle floating point data path.

The three grades [1x|2x|3x] of EdkDSP accelerator differ in HW-supported vector computing capabilities.

The area optimized accelerators **bce_fp11_1x1_0_plbw_v1_[10|11|12|13]_a** perform vector floating point operations FPADD, FPSUB.

The accelerators **bce_fp11_1x1_0_plbw_v1_[20|21|22|23]_a** perform vector floating point operations FPADD, FPSUB plus the vector floating point MAC operations for length of the vector 1 up to 10. These accelerators can be used in applications like floating point matrix multiplication with row and column dimensions <= 10.

The accelerators **bce_fp11_1x1_0_plbw_v1_[30|31|32|33]_a** support identical operations as the bce_fp11_1x8_0_plbw_v1_[20|21|22|23] plus the floating point vector by vector dot product computation with HW supported windup. It is optimized for computation FIR or LMS filter, each with size up to 250 coefficients. It is also effective in case of floating point matrix by matrix multiplications, where one of the dimensions is large (in the range from 11 to 255).

The four different configurations [x0|x1|x2|x3] of EdkDSP accelerator differ in HW supported I/O based on the PicoBlaze modules with firmware executed from the NV RAM.

The accelerators **bce_fp11_1x1_0_plbw_v1_[10|20|30]_a** have:
- No rotary encoder input PicoBlaze pre-processor and no I/O PicoBlaze pre-processor.
- No PicoBlaze controller for the LCD 2x32 character display.

The accelerators **bce_fp11_1x1_0_plbw_v1_[11|21|31]_a** have
- One rotary encoder input PicoBlaze pre-processor and one I/O PicoBlaze pre-processor.
- No PicoBlaze controller for the LCD 2x32 character display.

The accelerators **bce_fp11_1x1_0_plbw_v1_[12|22|32]_a** have:
- No rotary encoder input PicoBlaze pre-processor and no I/O PicoBlaze pre-processor.
- One PicoBlaze controller for the LCD 2x32 character display.

The accelerators **bce_fp11_1x1_0_plbw_v1_[13|23|33]_a** have
- One rotary encoder input PicoBlaze pre-processor and one I/O PicoBlaze pre-processor
- One PicoBlaze controller for the LCD 2x32 character display.

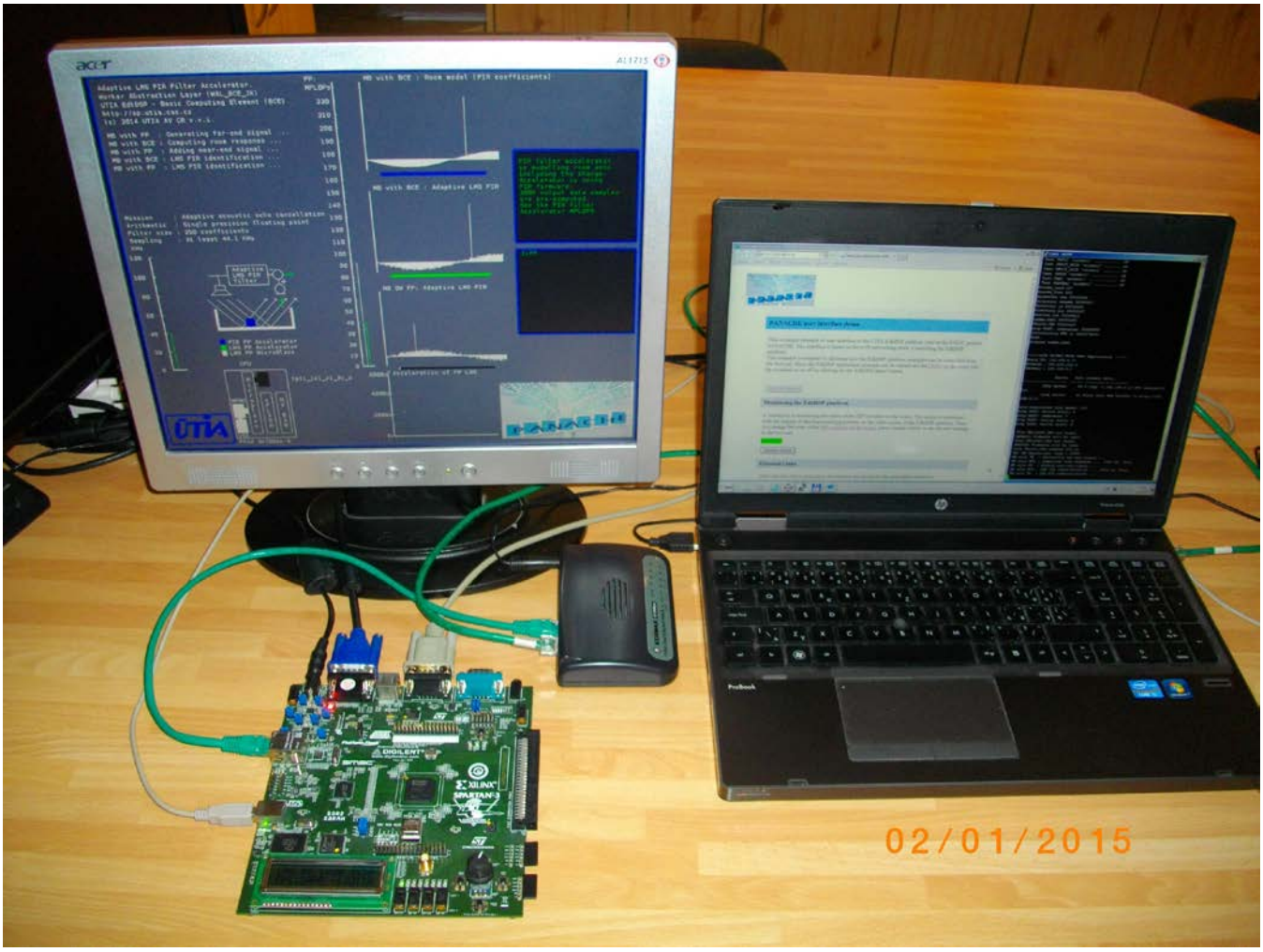

Figure 1: UTIA EdkDSP demonstrator with internet explorer GUI served from the 3S700AN kit

12 precompiled HW designs demonstrate use of single instance of UTIA EdkDSP floating point accelerator on 32bit PLB_v46 bus of the Xilinx MicroBlaze soft-core processor on the Xilinx Spartan SK 3AN700 FPGA board [6] with accelerator clock 75 MHz. See Figure 2.

Common properties of all 12 precompiled evaluation designs:

- The EdkDSP floating point accelerators are reconfigurable during runtime by change of firmware.
- 10/100 Mbit Ethernet point-to point connectivity with the PC.
- MicroBlaze system.
- Designed in Xilinx EDK/ISE 14.5 tools.
- Video display with fixed resolution 1024x768 70Hz with progressive scan. The video clock is 75 MHz
- Video display is supporting flat panel monitors with analogue VGA input (RGB, 4 bit per pixel).

Presented HW accelerators can results in better POWER per MFLOPS ratio for certain class of DSP applications in comparison to the computation on standard CPU with no floating point support. The demonstrator includes source code of set of SW demos prepared for compilation in the Xilinx SDK 14.5. The display controller is used to visualize the FIR RLS system parameter tracking by the recursive LMS algorithm. Results from accelerators are identical with the results computed by the MicroBlaze (with no floating point support). Video display is also demonstrating the measured acceleration of computation by this set of EdkDSP accelerators. See Figure 1, Figure 4 and Figure 6.

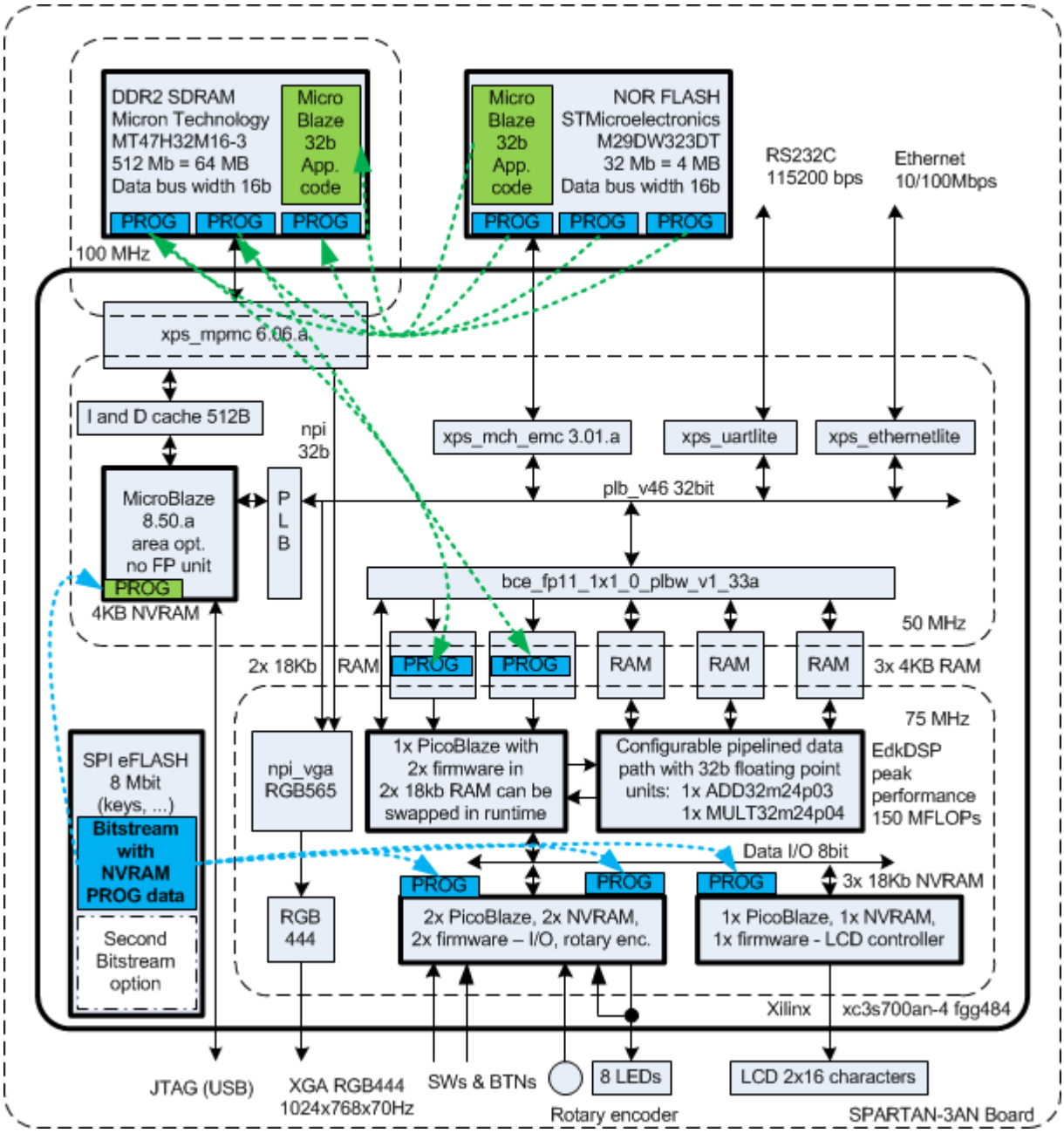

Figure 2: Architecture of EdkDSP designs on the 3S700AN board, xga75a_fp11_1x1_v1_33a.

Presented FPGA designs are running in the low-cost, Xilinx Spartan 3AN700 development board [6]. It is using the Micron Technology DDR2 SDRAM MT47H32M16-3 and the STMicroelectronics Parallel NOR Flash PROM M29DW3203DT. The memories are connected to Xilinx Spartan xc3s700an-4 fgg484 FPGA.

The DDR2 SDRAM maximal theoretical bandwidth is bandwidth is (100MHz*2B *2(DDR2)) = 400 MB/s.
The implemented designs require the DDR2 SDRAM bandwidth:
(50MHz*4B(MicroBlaze caches) + 75MHz*2B (RGB564 NPI port)) = 350 MB/s.

The 75 MHz EdkDSP subsystem contains 0-3 PicoBlaze processors [10] with programs in the NV RAM configured automatically from the eFLASH. Processors support processing of general I/O including the rotary encoder, and the 2 line, on board LCD display.

The rotary encoder processor is converting pulses coming from the rotary encoder (including the direction of the rotation) into an 8 bit world representing the position of the knob. The general I/O processor is converting the buttons, switches and data from the rotary encoder controller into the output to the LED on the board and for the EdkDSP PicoBlaze controller. See Figure 5 and Figure 7.

The LCD display controller is providing 32 8bit registers accessible for WR by the EdkDSP PicoBlaze controller. It is sending the content of these registers to the 4bit interface of the 2x16 character LCD display on board. See Figure 5 and Figure 7.

The 4-th PicoBlaze processor is reprogrammable and works with a complete Floating Point DSP unit, delivering sustained 92 MFLOP/s in case of FIR filter computation and 40 MFLOP/s in case of adaptive LMS filter application and data in the DDR2. Power consumption has been measured on the 1,2V FPGA core power line (<=240mA) and on the 5,0V line (<=460mA) powering complete board [6], (before all DC2DC power regulators). See Figure 3.

2.2 Resources used by the designs

The resources used by the 12 presented designs are summarised in Figure 3

3s700an-4 fgg484	fp add mul	fp mac	fp prod	User IO rot enc	User IO lcd dis	Design size ff %	Design size lut %	Design size bram no(of)	Design size slice %	Core 1,2V mA	Board 5,0V mA	Performance LMS mflop	Performance FIR mflop
xga75a_fp11_1x1_v1_10a	x					53	74	17(20)	94	200	450		
xga75a_fp11_1x1_v1_11a	x			2x		55	78	19(20)	96	220	450		
xga75a_fp11_1x1_v1_12a	x				x	53	76	18(20)	96	210	450		
xga75a_fp11_1x1_v1_13a	x			2x	x	56	80	20(20)	97	230	450		
xga75a_fp11_1x1_v1_20a	x	x				54	86	17(20)	97	190	450		
xga75a_fp11_1x1_v1_21a	x	x		2x		56	81	19(20)	98	230	450		
xga75a_fp11_1x1_v1_22a	x	x			x	55	78	18(20)	97	220	450		
xga75a_fp11_1x1_v1_23a	x	x		2x	x	57	82	20(20)	97	230	450		
xga75a_fp11_1x1_v1_30a	x	x	x			56	81	17(20)	98	200	460	**40**	**92**
xga75a_fp11_1x1_v1_31a	x	x	x	2x		58	85	19(20)	98	220	460	**40**	**92**
xga75a_fp11_1x1_v1_32a	x	x	x		x	56	83	18(20)	98	240	460	**40**	**92**
xga75a_fp11_1x1_v1_33a	x	x	x	2x	x	59	87	20(20)	99	230	460	**40**	**92**

Figure 3: MicroBlaze 50 MHz; EdkDSP 75 MHz; PicoBlaze I/O processors with NV RAM

2.3 Re-programmability of EdkDSP accelerators

The 75 MHz EdkDSP floating point accelerator subsystem contains one reprogrammable Xilinx PicoBlaze processor and the reconfigurable floating point data path. It is delivering sustained 92 MFLOP/s in case of 250 tap FIR filter computation and 40 MFLOP/s in case of the adaptive 250 tap LMS filter identification on the 3S700AN. The Xilinx PicoBlaze processor has fixed configuration with size of the program memory 1024 (18 bit wide) words, 64 Bytes scratch pad RAM memory and the interrupt vector in the address 1023.All EdkDSP accelerator designs present in this package instantiate 2 program memories, each with the 1024 (18bit wide) words. Both program memories are accessible by MicroBlaze processor via PLB bus. The PicoBlaze can execute program from each of these memories. The MicroBlaze application can write new firmware to the currently unused program memory, while the PicoBlaze is executing firmware from the other program memory.

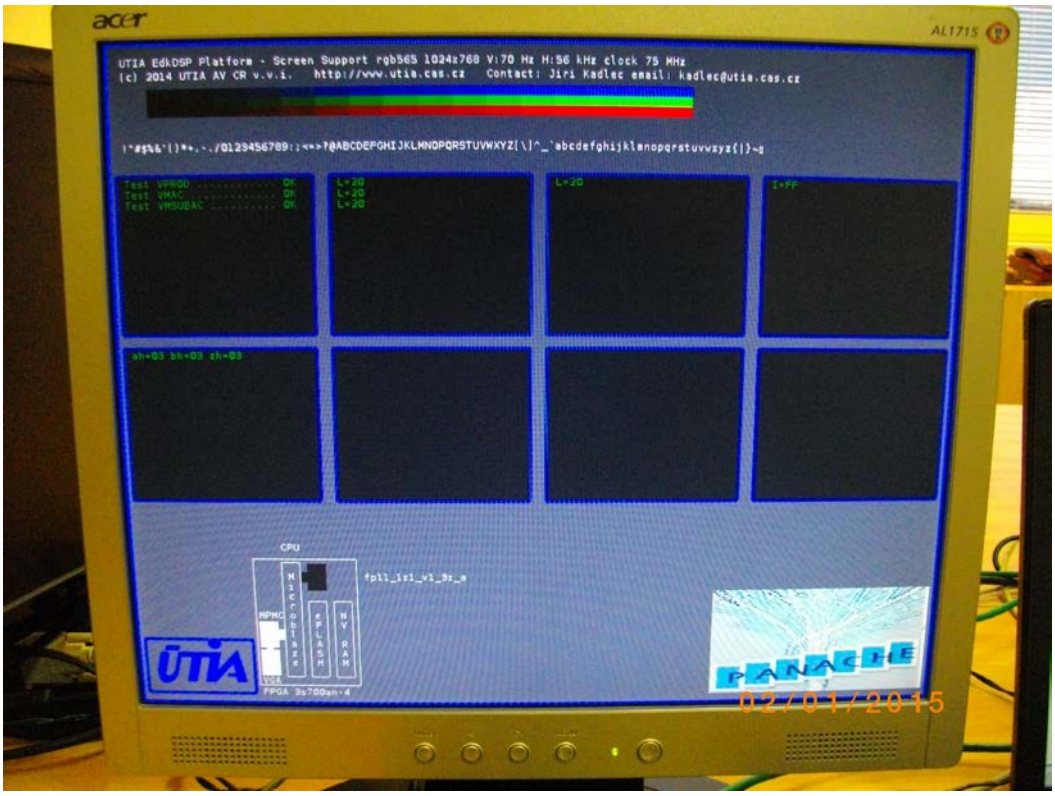

Figure 4: XGA 1024x768p70 screen output of 3S700AN. Demo is testing all FP vector operations.

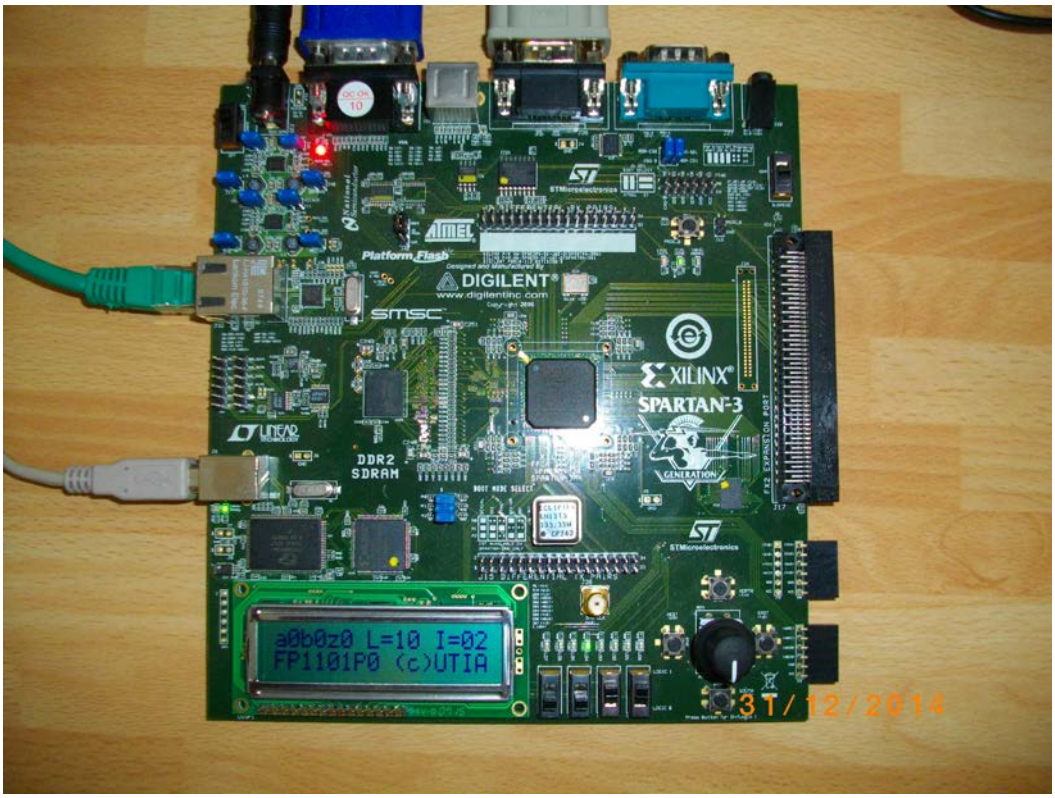

Figure 5: 3S700AN 2-line LCD output. Demo is testing all FP vector operations

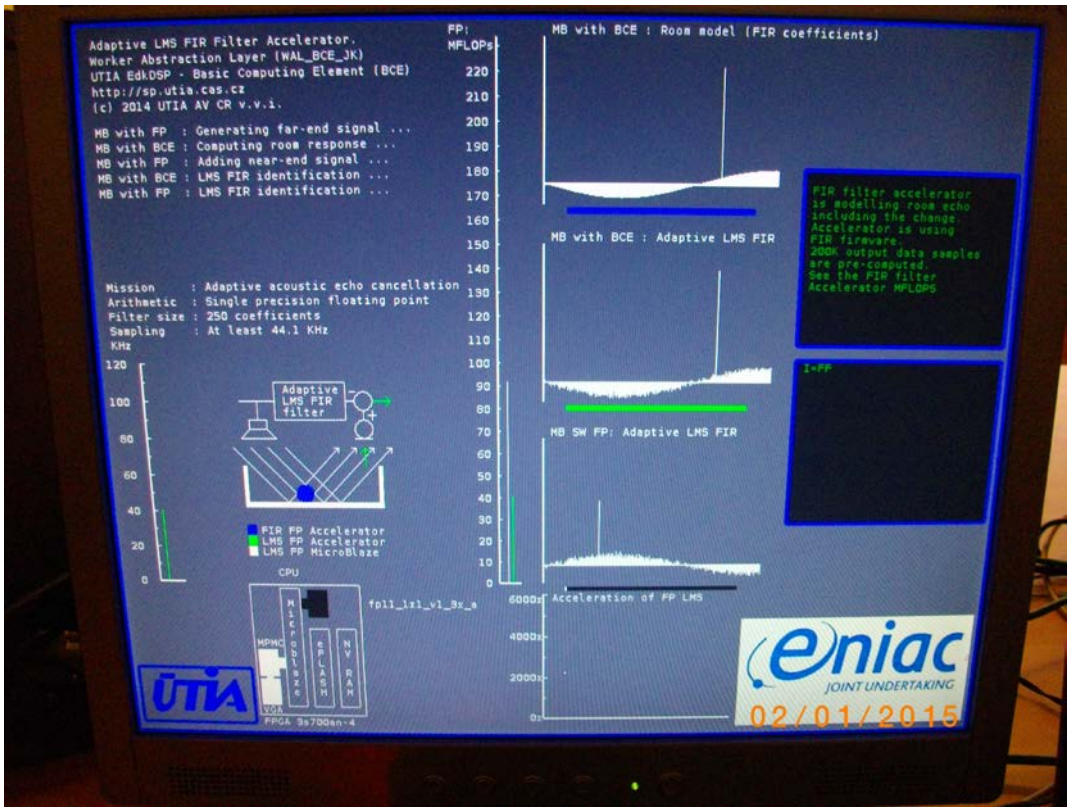

Figure 6: EdkDSP demonstrator; FIR filter 92 MFLOPS; adaptive LMS filter 40 MFLOPS

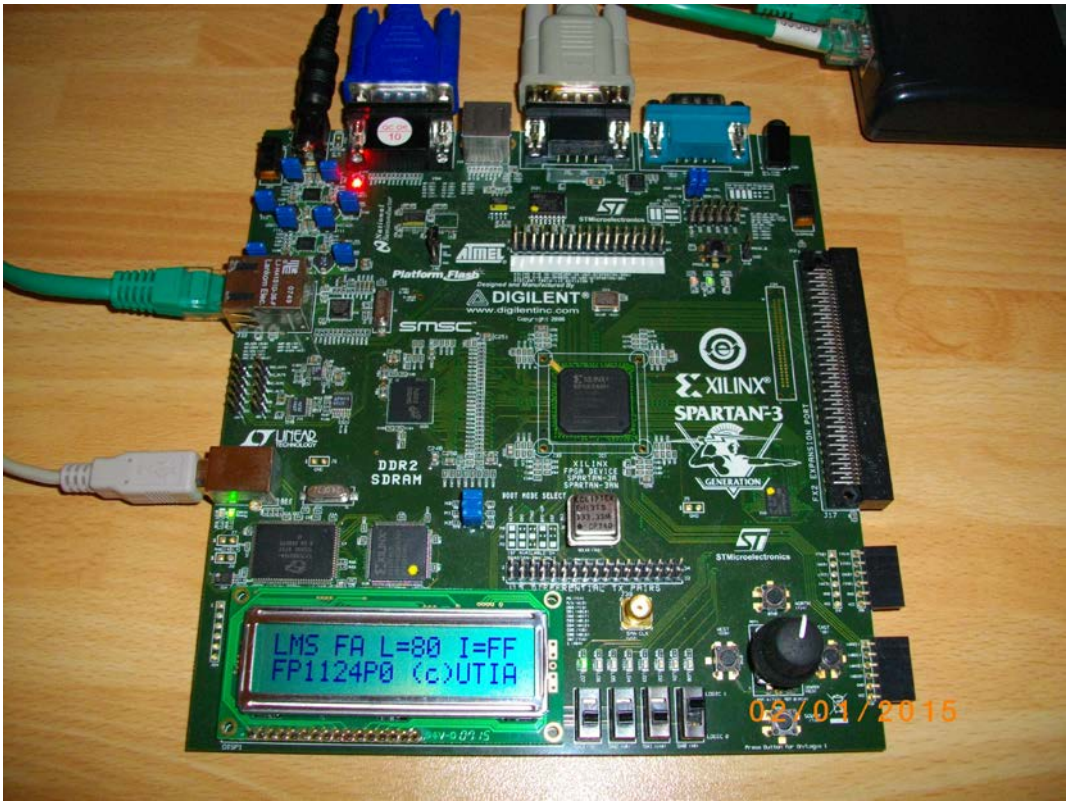

Figure 7: 3S700AN 2-line LCD output. Demo of the floating point FIR and adaptive LMS filters.

3. Installation of the EdkDSP platform on 3S700AN board

3.1 Import of precompiled projects and SW into Xilinx SDK 14.5

Unzip the evaluation package to directory of your choice. The directory c:\VM_07 will be used in this application note. You will get these directories:

```
c:\VM\d_145_3an_plb
29.12.2014  21:03    <DIR>          .
29.12.2014  21:03    <DIR>          ..
29.12.2014  21:02    <DIR>          d_3s700an_xga75a_fp11_1x1
29.12.2014  21:02    <DIR>          d_3s700an_xga75a_fp11_1x1_IMPORT
29.12.2014  21:02    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_10_a
29.12.2014  21:02    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_11_a
29.12.2014  21:02    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_12_a
29.12.2014  21:02    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_13_a
29.12.2014  21:02    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_20_a
29.12.2014  21:03    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_21_a
29.12.2014  21:03    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_22_a
29.12.2014  21:03    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_23_a
29.12.2014  21:03    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_30_a
29.12.2014  21:03    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_31_a
29.12.2014  21:03    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_32_a
29.12.2014  21:03    <DIR>          d_3s700an_xga75a_fp11_1x1_v1_33_a
```

Select SDK 14.5 workspace in c:\VM_07\d_145_3an_plb\d_3s700an_xga75a_fp11_1x1\SDK_Workspace.

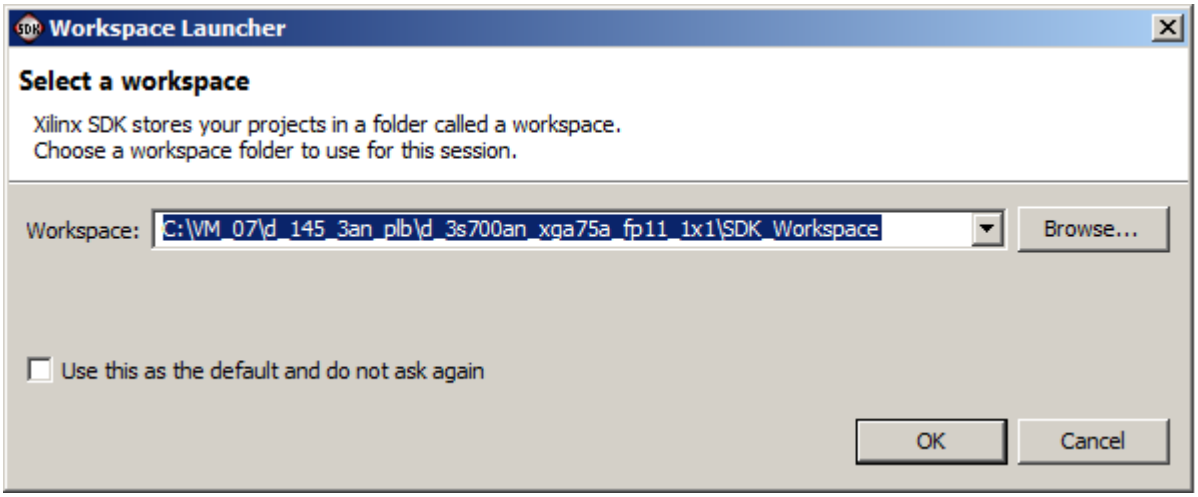

Figure 8: Select the SDK 14.5 Workspace

Add path to the UTIA EdkDSP repository of SW drivers and path to the Xilinx repository of SW drivers c:\VM_07\d_145_3an_plb\d_3s700an_xga75a_fp11_1x1\repo_edkdsp.

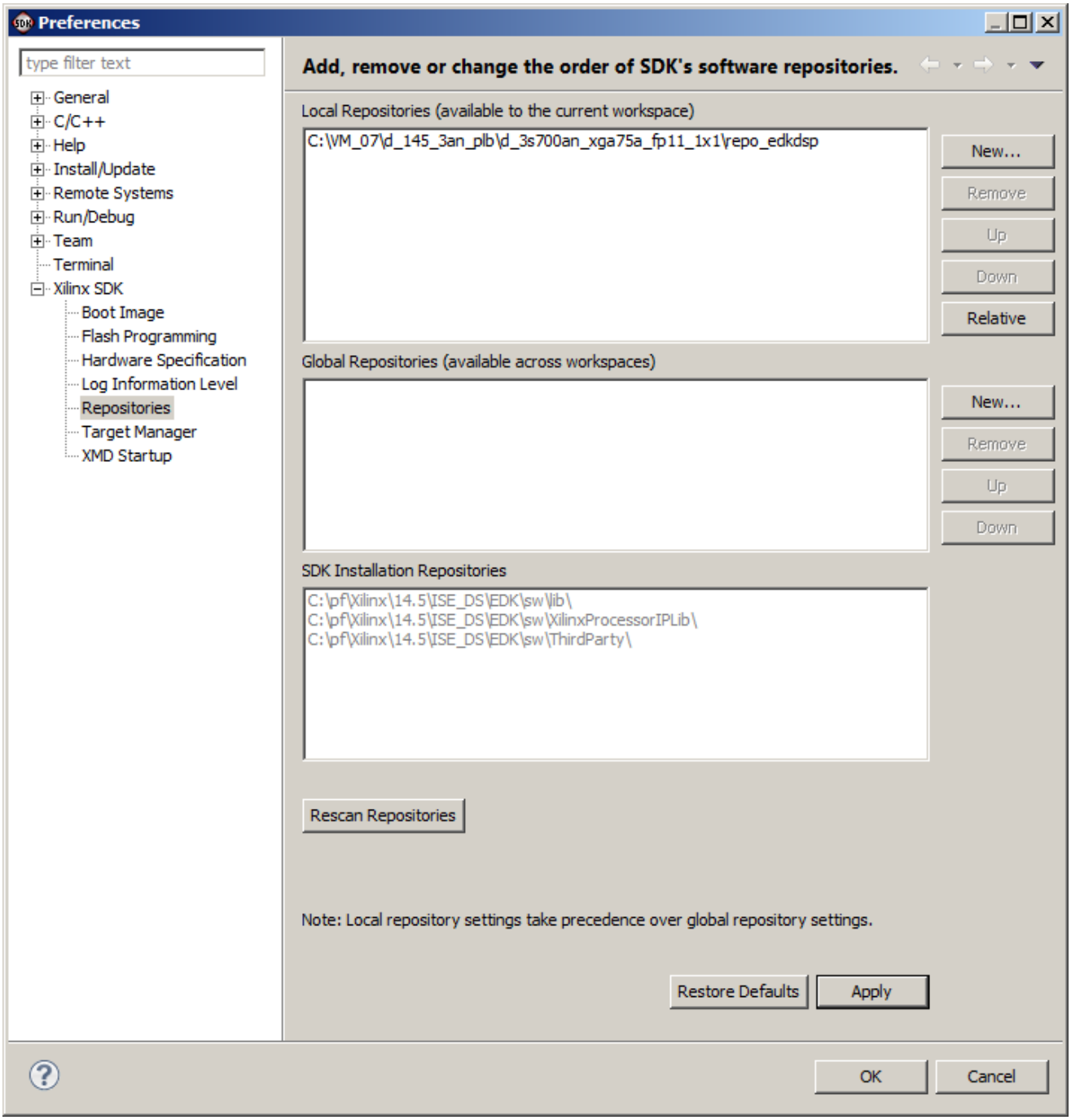

Figure 9: Include the Xilinx SW repository and the UTIA EdkDSP SW repository

Click on the “Rescan Repositories” button. Click on the “Apply button”, and finally click on the OK button. The paths to the SW drivers have been defined.

In SDK, select File -> New -> Project … -> Xilinx -> Hardware Platform Specification.
Click on the Next button.

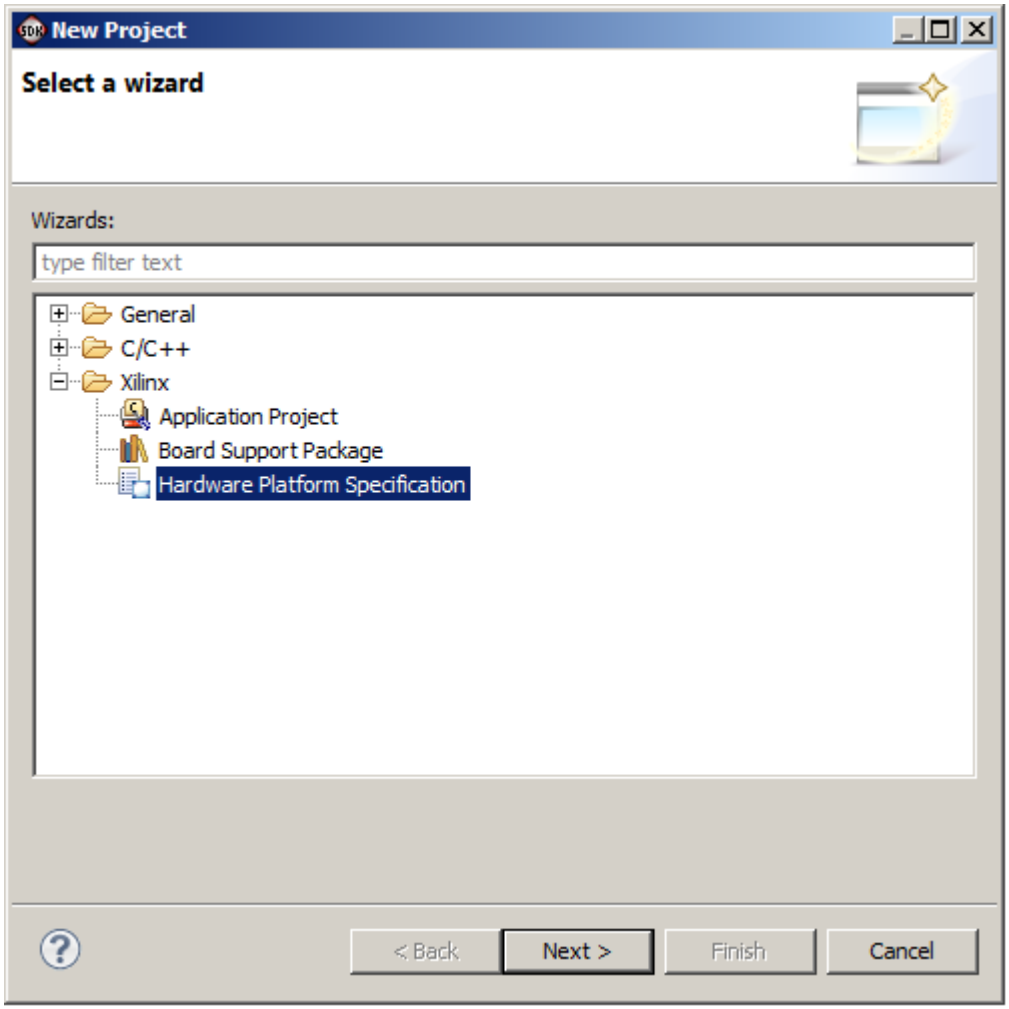

Figure 10: Specify the Hardware Platform

In the “New Hardware Project” screen, fill into the Project name:
hw_platform_0

In the New Hardware Project screen, fill into the Target Hardware Specification:

C:\VM_07\d_145_3an_plb\d_3s700an_xga75a_fp11_1x1_v1_33a\SDK_Export\hw\system.xml

This will specify one of the 12 precompiled HW designs present in the evaluation package.
We have selected design demonstrating the UTIA EdkDSP accelerator, with floating point single data path, with 75 MHz clock, rotary encoder controller and LCD display controller in the evaluation netlist bce_fp11_1x1_0_plbw_v1_33_a.

Click on “Finish” button to finalize the selection of the precompiled HW design.

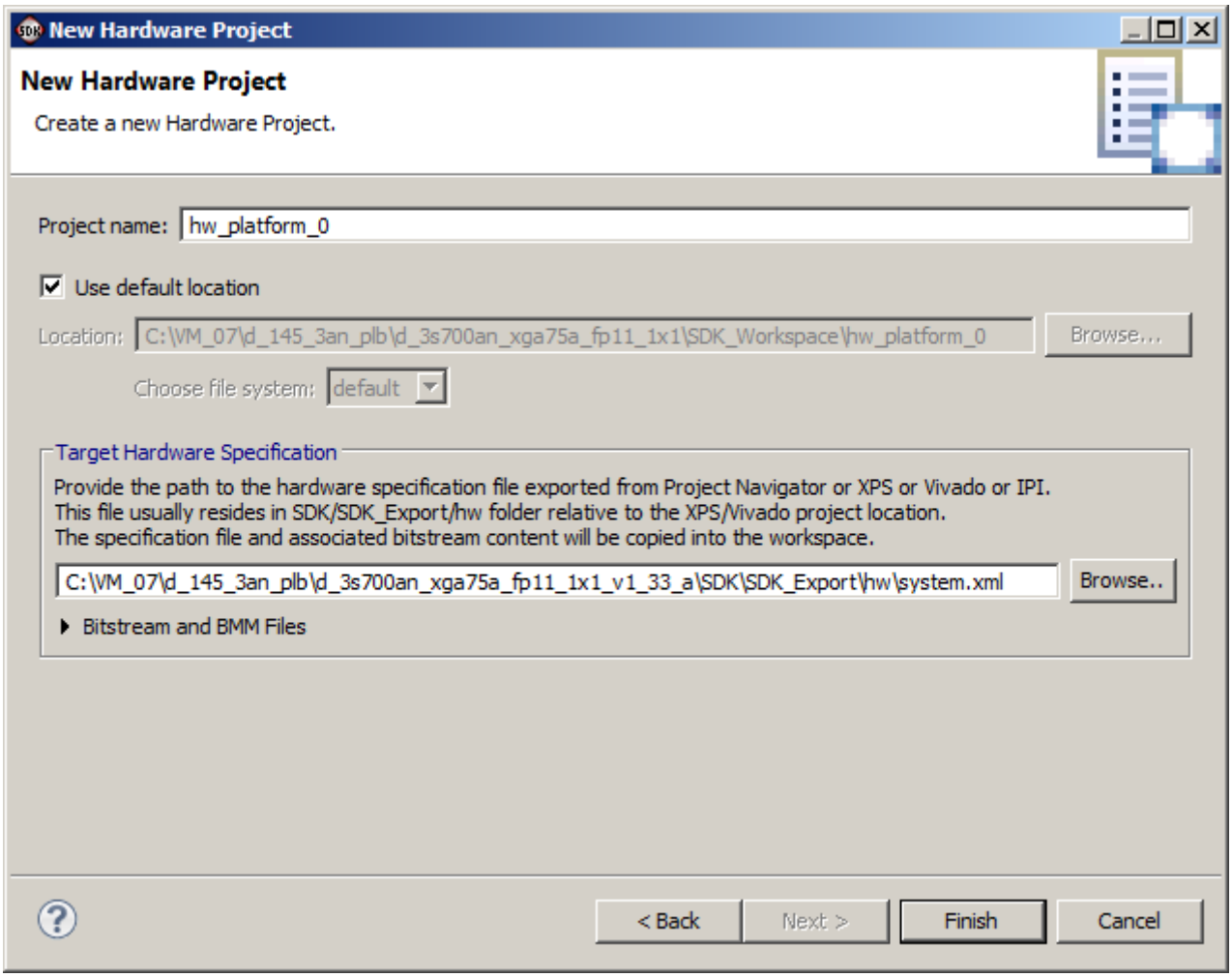

Figure 11: Use the name "hw_platform_0" and selet one of the provided xml design descriptions

The hardware platform "hw_platform" has been created.

SDK is interpreting the system.xml and presents HW cores of in the design. See Figure 11.

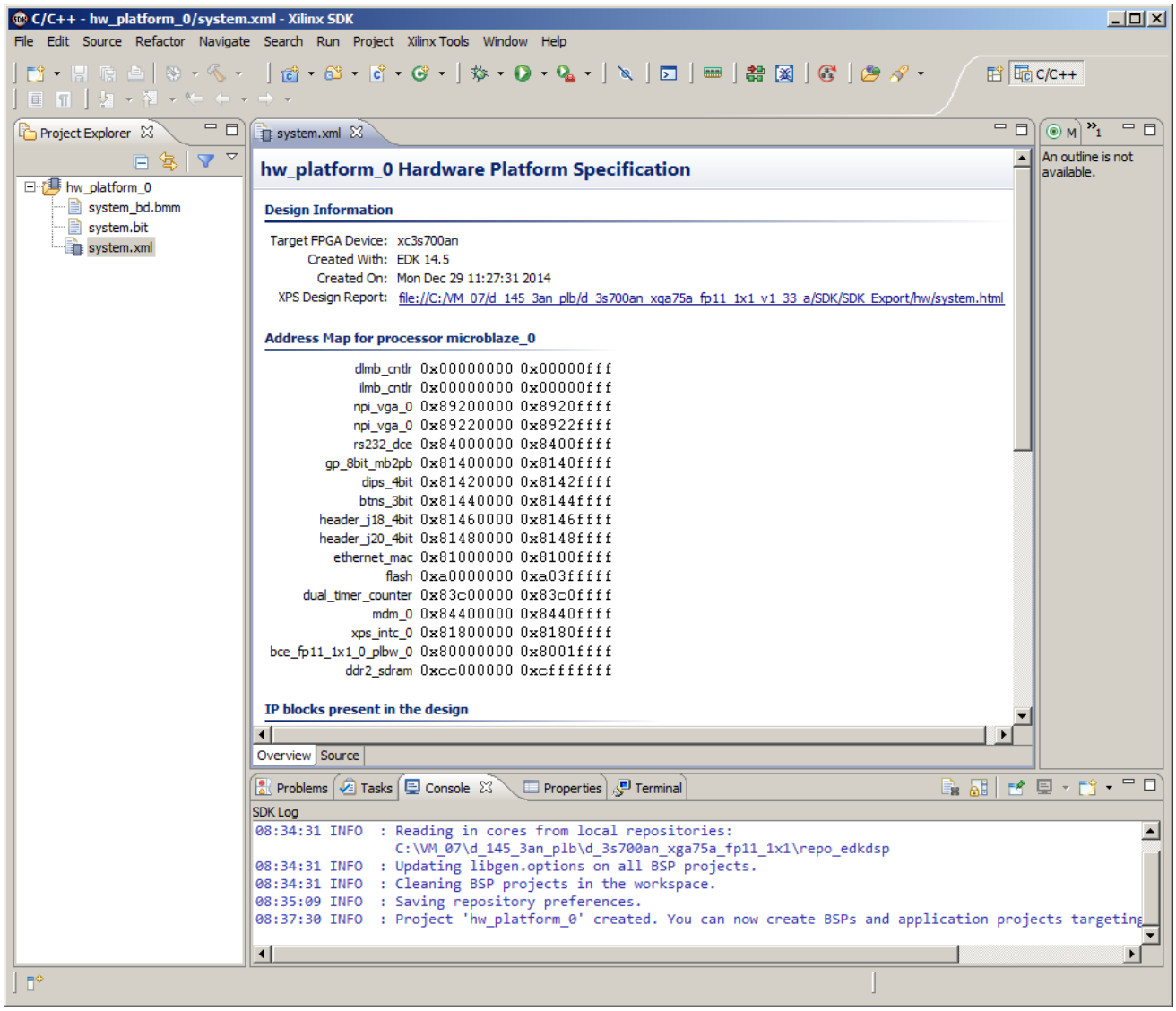

Figure 12: Hardware platform with the MicroBlaze address map

SW projects can be imported into SDK now. Select:

File -> Import -> General -> Existing Projects into Workspace
Click on Next button. See Figure 12.

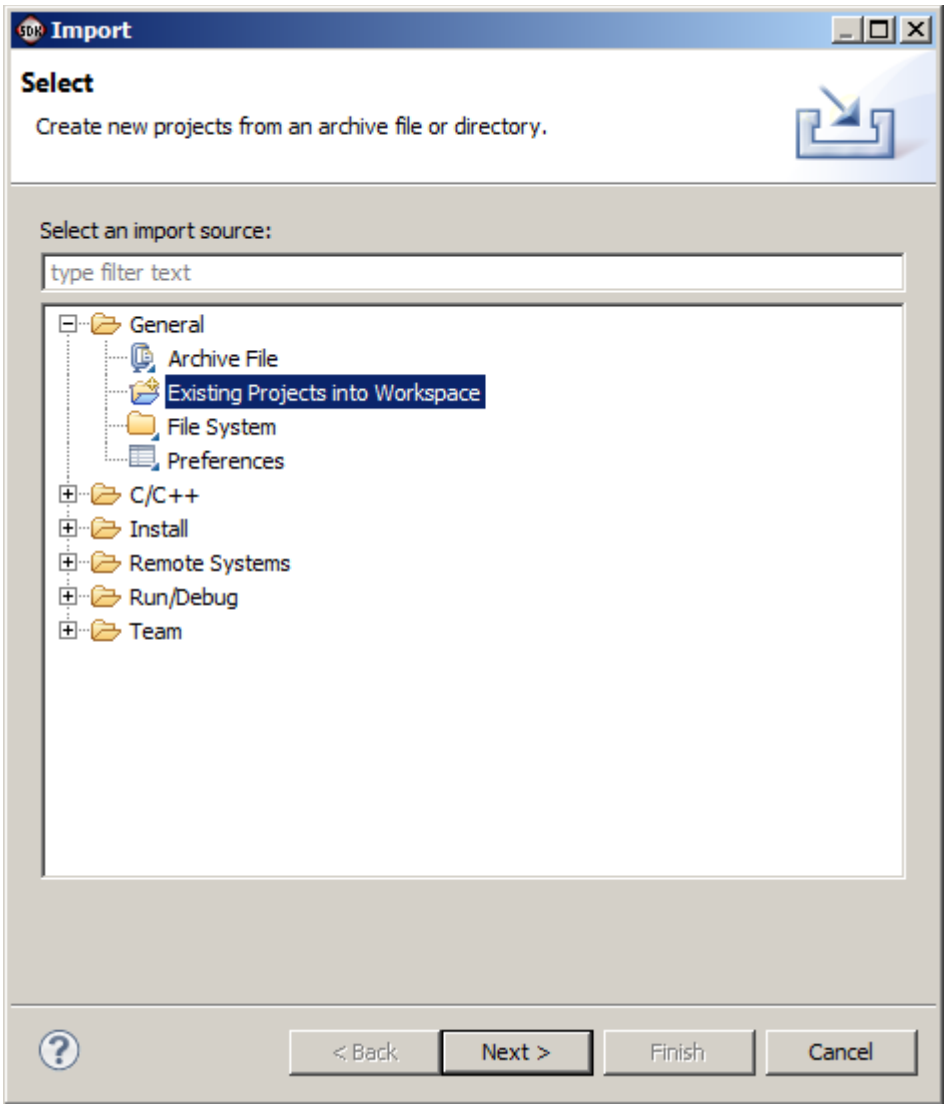

Figure 13: Import existing projects into Workspace

Type directory with projects to be imported. See Figure 13.

C:\VM_07\d_145_3an_plb\d_3s700an_xga75a_fp11_1x1_IMPORT

Set the “Copy projects into workspace” check box.
Click on Finish button. See Figure 13.

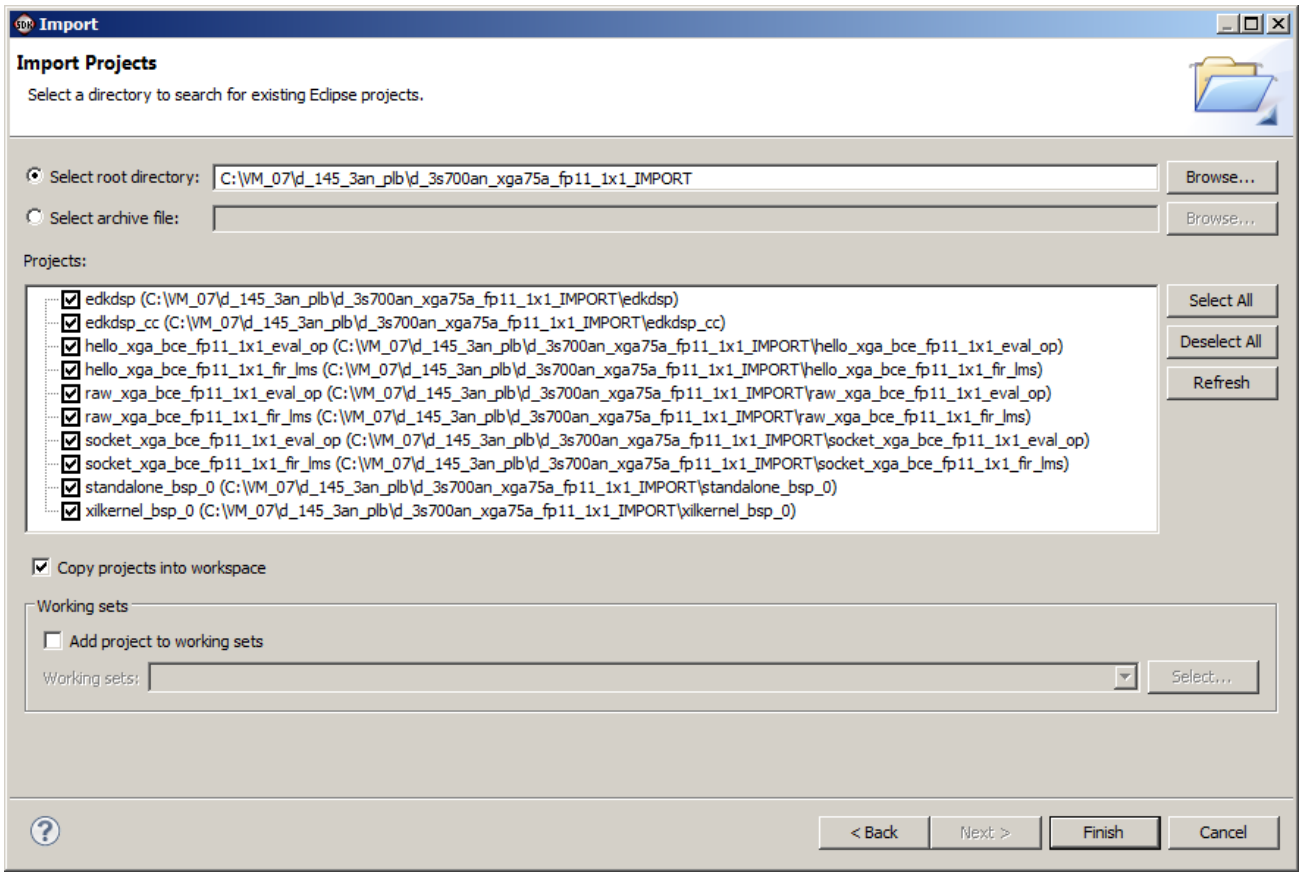

Figure 14: Select 'Copy projects into workspace' and click 'Finish' to import projects.

All the UTIA EdkDSP SW projects are imported into SDK workspace from the directory C:\VM_07\d_145_3an_plb\d_3s700an_xga75a_fp11_1x1_IMPORT
Process of compilation will start automatically.

This first compilation of all SDK SW projects can take several minutes to finish. It should finish without errors. See Figure 14.

3.2 Description of EdkDSP project

See content of the introductory “edkdsp” project in the “Project Explorer” window of the SDK. Inspect also the list of IP blocks and related driver versions present in the evaluation design. See Figure 14.

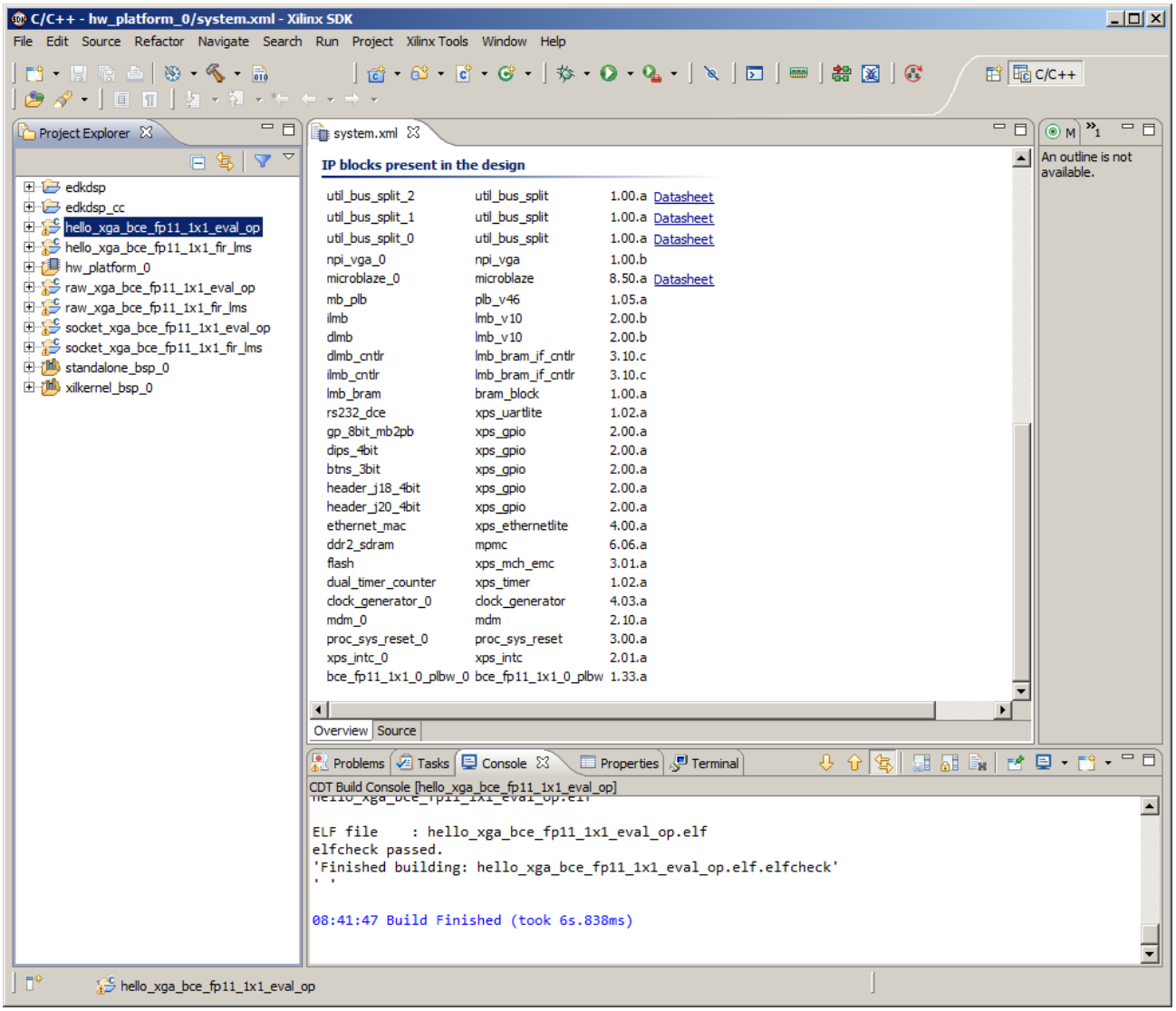

Figure 15: All projects are compiled. Open the “edkdsp” introduction SW project.

The introductory “edkdsp” project is using only the serial link terminal and the Xilinx memory based file system. It is not using the LwIP Ethernet libraries and it is not using the video display.

Connect the jtag and serial line USB cables to your 3S700AN board and switch ON the board.

Start serial line terminal on your PC. See configuration of terminal PuTTY on Figure 15.

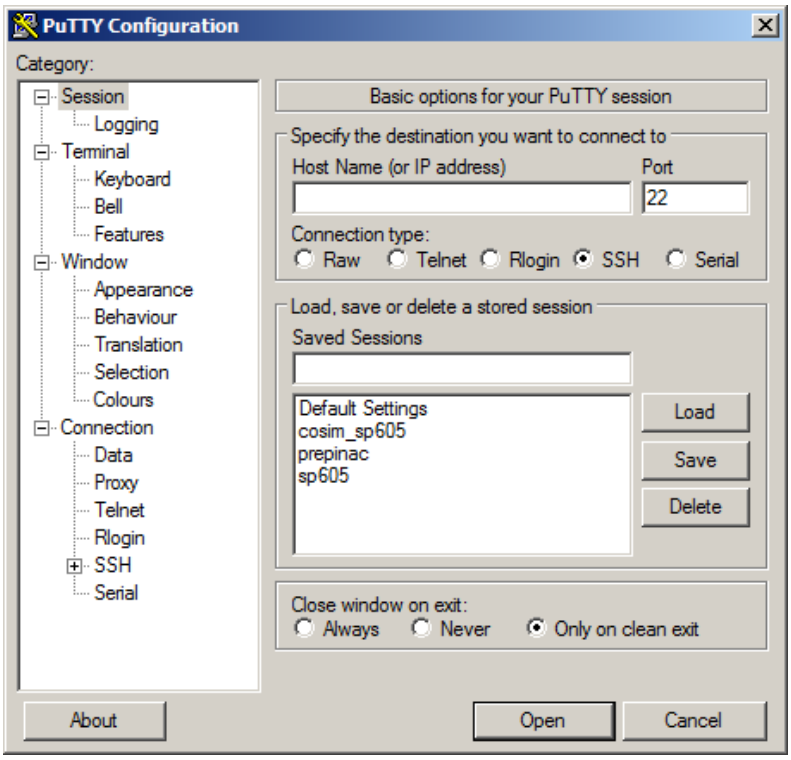

Figure 16: Start the serial line terminal (PuTTY)

Select 115200 baud and “Flow control” to None. See Figure 16 and Figure 17.

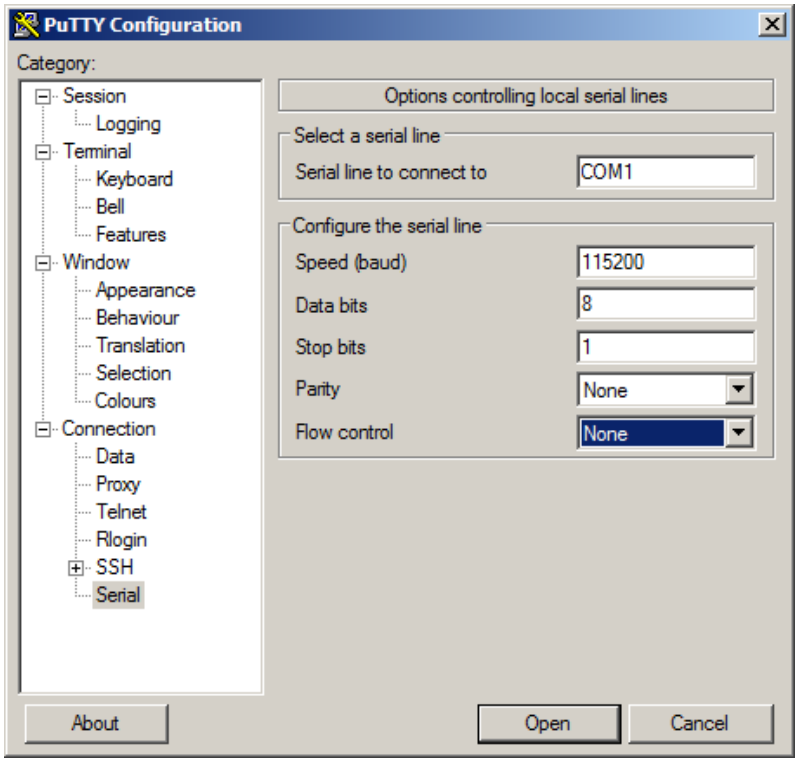

Figure 17: Setup your actual COM port, Speed 115200 baud, and Flow control ”None”

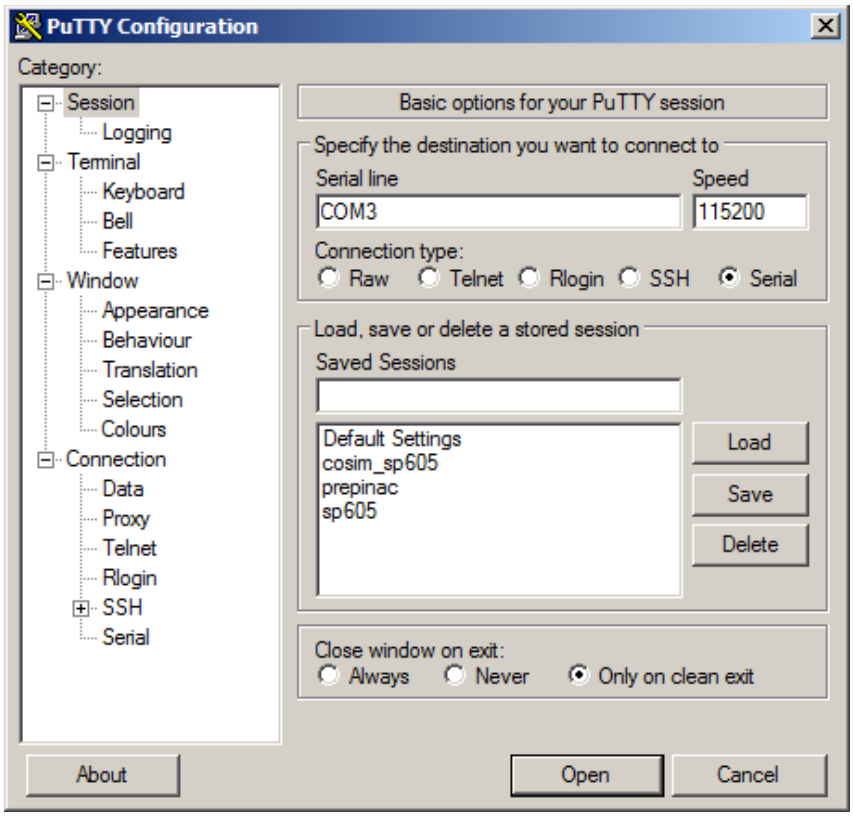

Figure 18: Select "Serial" Session and the terminal window will open.

In SDK, program the 3S700AN board by selecting:
Xilinx Tools -> Program FPGA

Type or browse to the "system.bit" file and the "system_bd.bmm" file:

C:\VM_07\d_145_3an_plb\d_3s700an_xga75a_fp11_1x1\SDK_Workspace\hw_platform\system.bit
C:\VM_07\d_145_3an_plb\d_3s700an_xga75a_fp11_1x1\SDK_Workspace\hw_platform\system_bd.bmm

Click on the "Program" button.

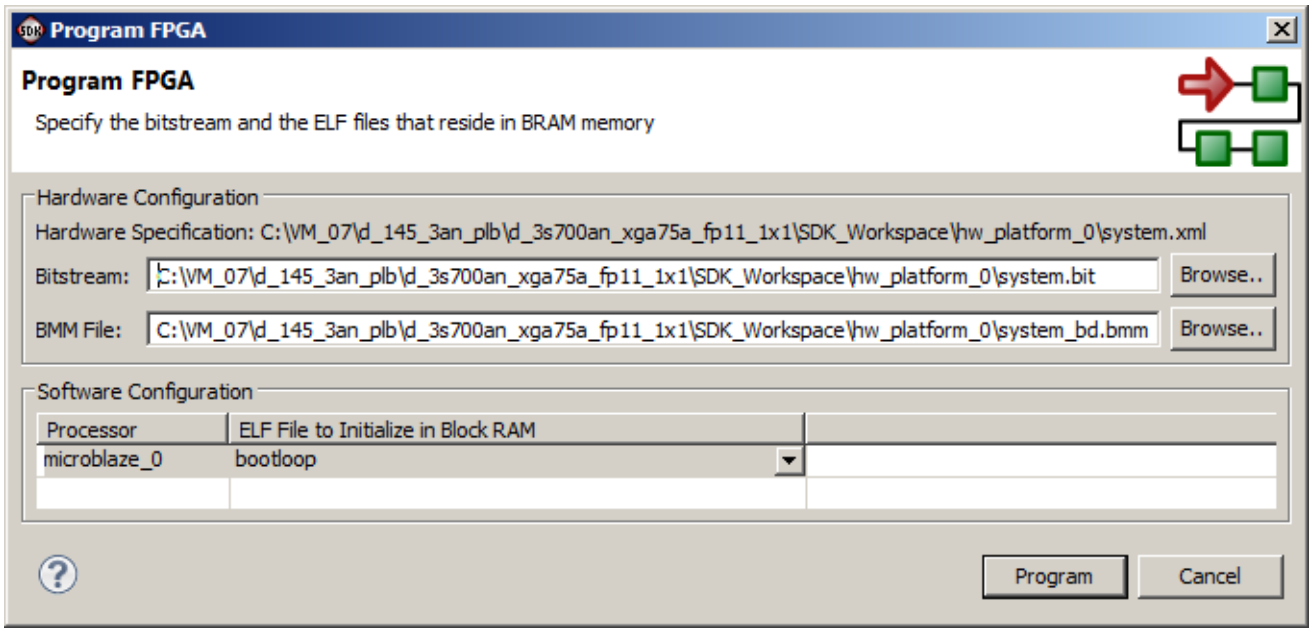

Figure 19: Specify the .bit and the .bmm file with location of the NV RAM for the MB program.

The 3S700AN board is programmed with the .bit file now. The MicroBlaze is running in the initial bootloop.

The SW application from the edkdsp project has to be downloaded to the DDR3 memory, now.
The "edkdsp_introduction.c" application is performing these steps:

- Initialize cache and serial line controller.
- Initialize memory based file system from data linked in the .elf binary file.
- Initialize data structures describing the edk_fp12_1x8_v1_40_a accelerator.
- Write firmware to both program memories of the accelerator.
- Read properties and the license status of the accelerator.
- MicroBlaze application can identify which member of the accelerator family is actually present (10|20|30|40) and if the floating point pipelined divider data path is present or not.
- Test floating point vector addition computed in the accelerator with 8xSIMD data path.
    - Communicate from the accelerator data about input and led I/O to MicroBlaze.
    - Write these data to an ascii text file in the ram based file system and to the terminal.
- Verify the floating point results in MicroBlaze.
- Print to the terminal the number of free and used data blocks.
- Print list of top level directories present in the file system.

Select the "edkdsp" project by clicking on it in the SDK Project Explorer Window.

In SDK, select:
Run -> Debug Configuration ->Xilinc C/C++ ELF

Click on the "New launch configuration" in the Run configuration screen and the "edkdsp" project executable Debug\edkdsp.elf Is ready for download to DDR3 on the 3S700AN board via the jtag cable.
Click on "Debug" button to download the executable and start the debugger. See Figure 19.
Click on "Yes" in the pop up window related to the switch to the Debug perspective.

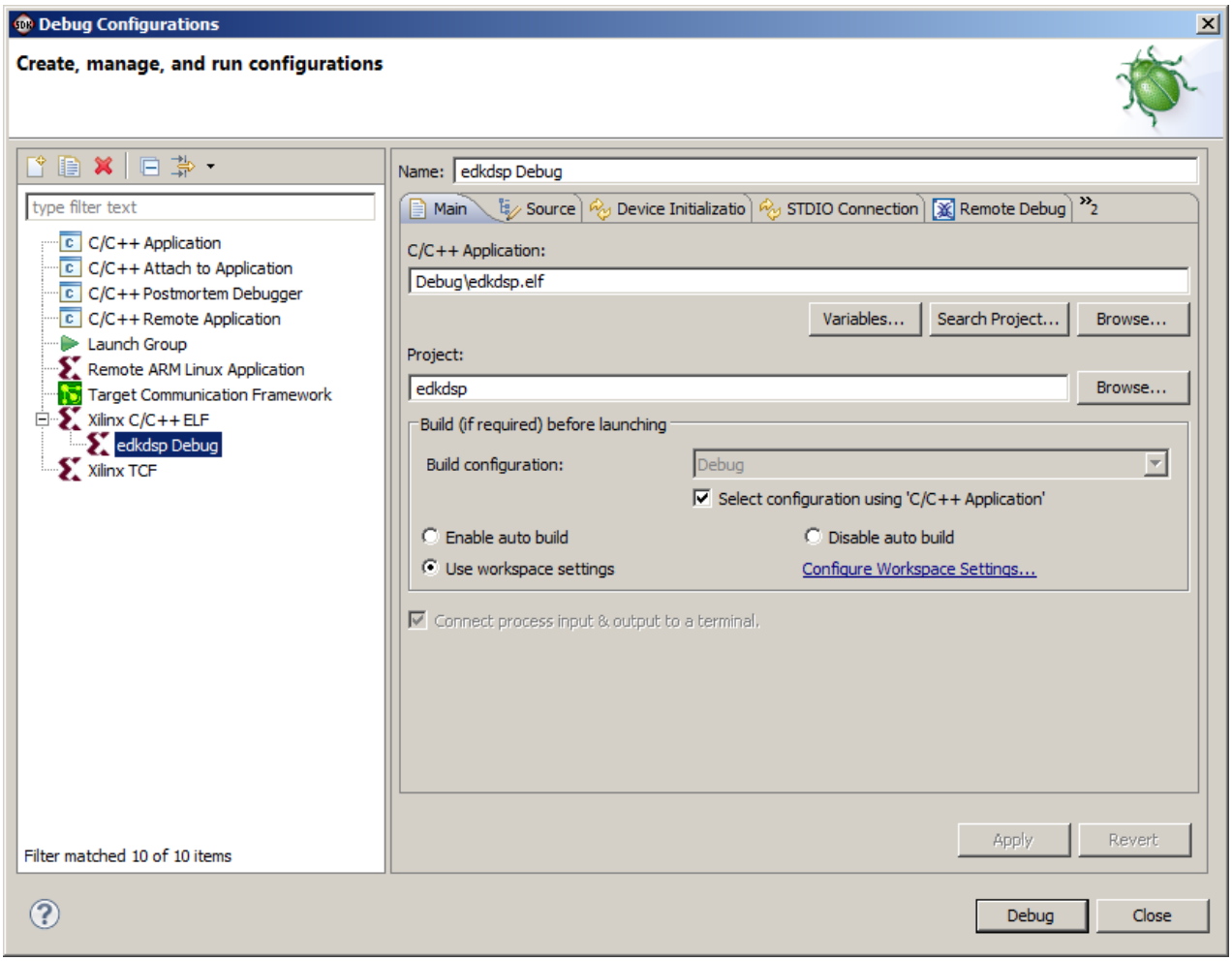

Figure 20: Debug "edkdsp.elf" code on MicroBlaze

The Debug\edkdsp.elf is executed up to the breakpoint on the first executable C code. See Figure 21.

Select next breakpoint as indicated in Figure 22 and click on Resume (F8) icon to run up to this new breakpoint located inside of the triple loop on the call to the function
`bce_fp11_1x1_VADD (worker1, capabilities1, ah, bh, zh);`

Processor stops on the breakpoint and terminal is indicating properties of the accelerator. See Figure 23.

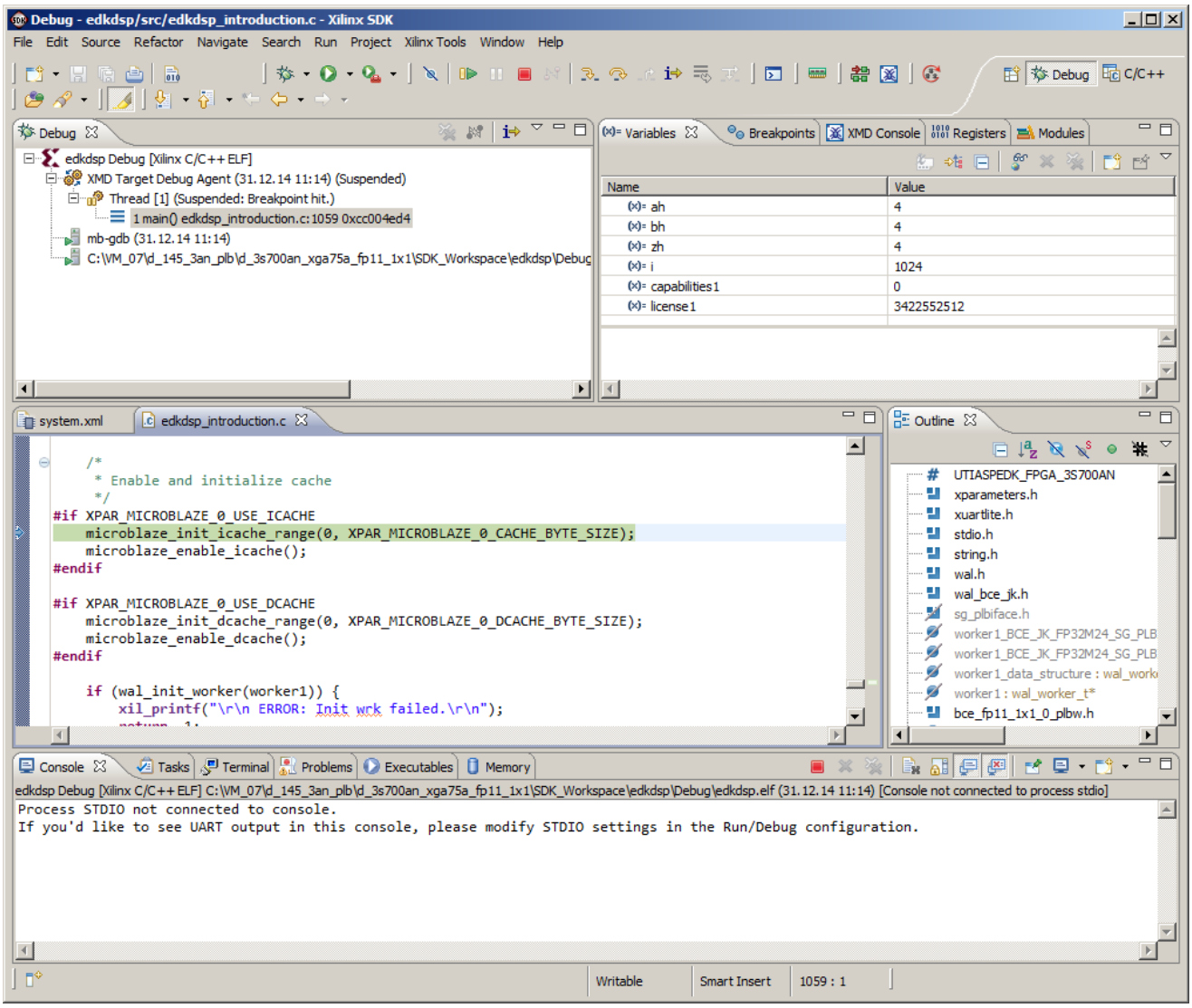

Figure 21: The debugger stops on the first executable line of MicroBlaze C code.

Click on the on Resume (F8) icon to execute the the test function with parameters ah=0, bh=0, zh=0. See the console output.

Click again the on Resume (F8) icon to execute the test function with parameters ah=0, bh=0, zh=1. See the console output as indicated in Figure 24.

Remove the breakpoint and click on the on Resume (F8) icon to execute the program up to the end.
The debugger stops at the end of the program. Terminate the debugger and close the debug perspective and return to the default SDK C/C++ perspective. The Debug\edkdsp.elf is running until you click on the “Remove launch” (X) in the SDK.

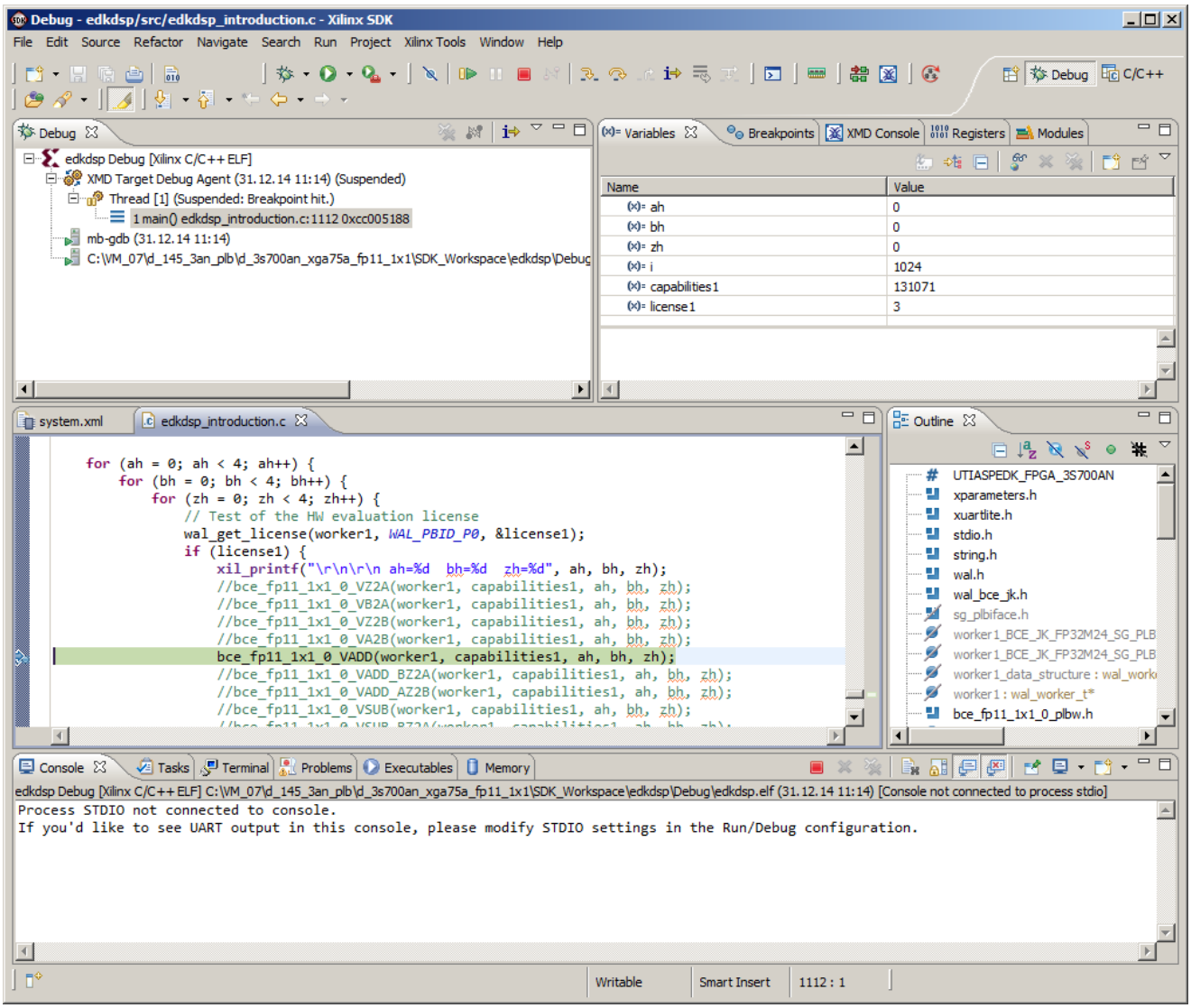

Figure 22: Set the breakpoint on function bce_fp11_1x1_0_VADD() testing the vector floating point ADD operation.

.

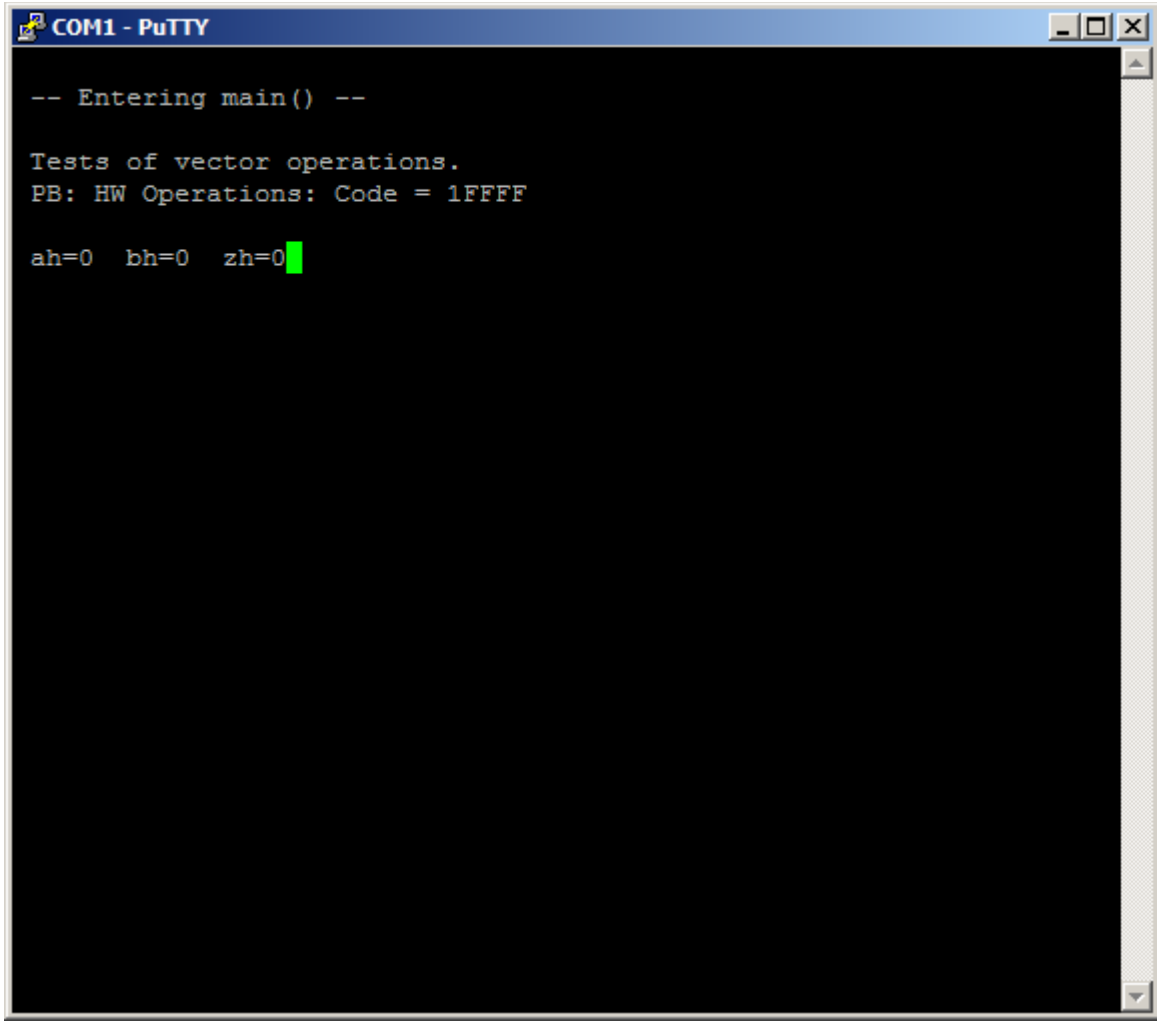

Figure 23: The application "edkdsp" stopped on initial breakpoint.

Compare the MicroBlaze source code "edkdsp\src\edkdsp_introduction.c" in the SDK project "edkdsp" together with the PicoBlaze controller firmware edkdsp_cc\a\a_fp1101p0.c in the accelerator. See Figure 25.

It is demonstrating, how the MicroBlaze processor communicates with the PicoBlaze controller present in the accelerator. The MicroBlaze C WAL library functions support the exchange of floating point data in DDR2 (C variables and arrays) to three dual-ported 4 kB memories A1, B1, Z1 of the accelerator. MicroBlaze can access these memories via its PLB interface. Each memory is organised as 4 banks of 256 32 bit words. See the block diagram on Figure 2. The PicoBlaze controller is executing binary firmware corresponding to program edkdsp_cc\a\a_fp1101p0.c. It is controlling the configurable, floating point, data flow unit. The data flow unit has HW supported access to read and write and into the three 4 kB memories A1, B1, Z1 from the accelerator ports with programmable auto-increment of addresses.

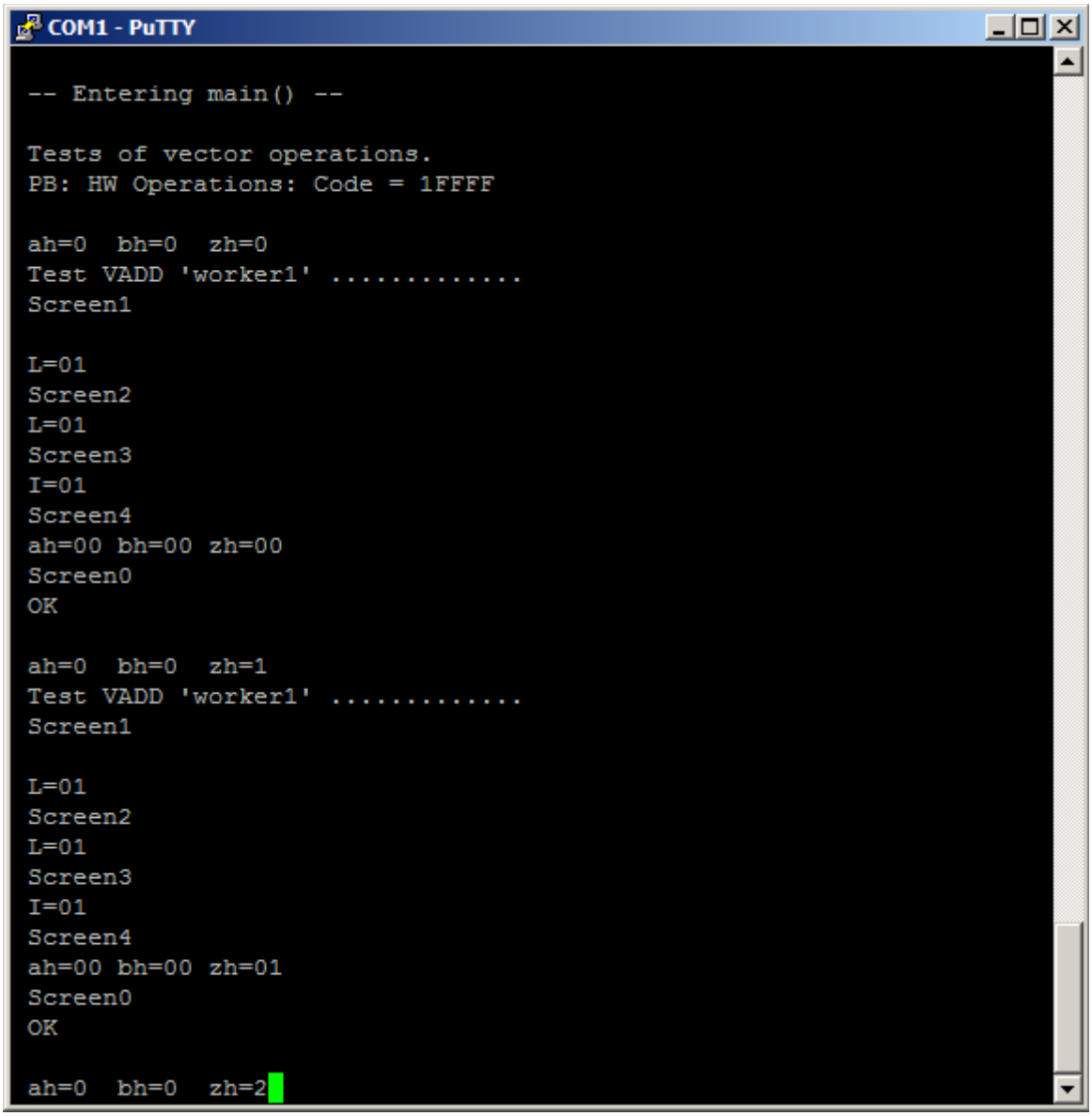

Figure 24: Terminal after the second call to the tested bce_fp11_1x1_0_VADD() function.

The listing on Figure 25 is indicating, how the MicroBlaze "edkdsp_introduction.c" program cooperates with the PicoBlaze firmware program edkdsp_cc\a\fp1101p0.c. It presents the initial sequence of the PicoBlaze firmware program edkdsp_cc\a\a_fp1101p0.c. The function **pb2dfu_set (C_DFU_OP, op)** starts the vector floating point operation of the data flow unit of the accelerator. See Figure 25. PicoBlaze C code is synchronised with the result of the vector floating point operation of the 8xSIMD data flow unit in function call **function pb2dfu_wait4hw ()**. See Figure 25.

PicoBlaze also reads the LED information produced by the dedicated PicoBlaze processors for a rotary encoder input in cooperation with the I/O PicoBlaze pre-processor. The PicoBlaze firmware program edkdsp_cc\a\a_fp1101p0.c communicates I/O data to the MicroBlaze. It also writes the information about the progress of computation to the LCD 2x 16 character display via the dedicated PicoBlaze controller. See Figure 2. The 3 controllers execute fixed firmware from the NV RAMs. Each NV RAM is initialised in the power-up configuration phase from the bitstream. The bitstream is read by the 3S700AN chip from its internal eFLASH [5].

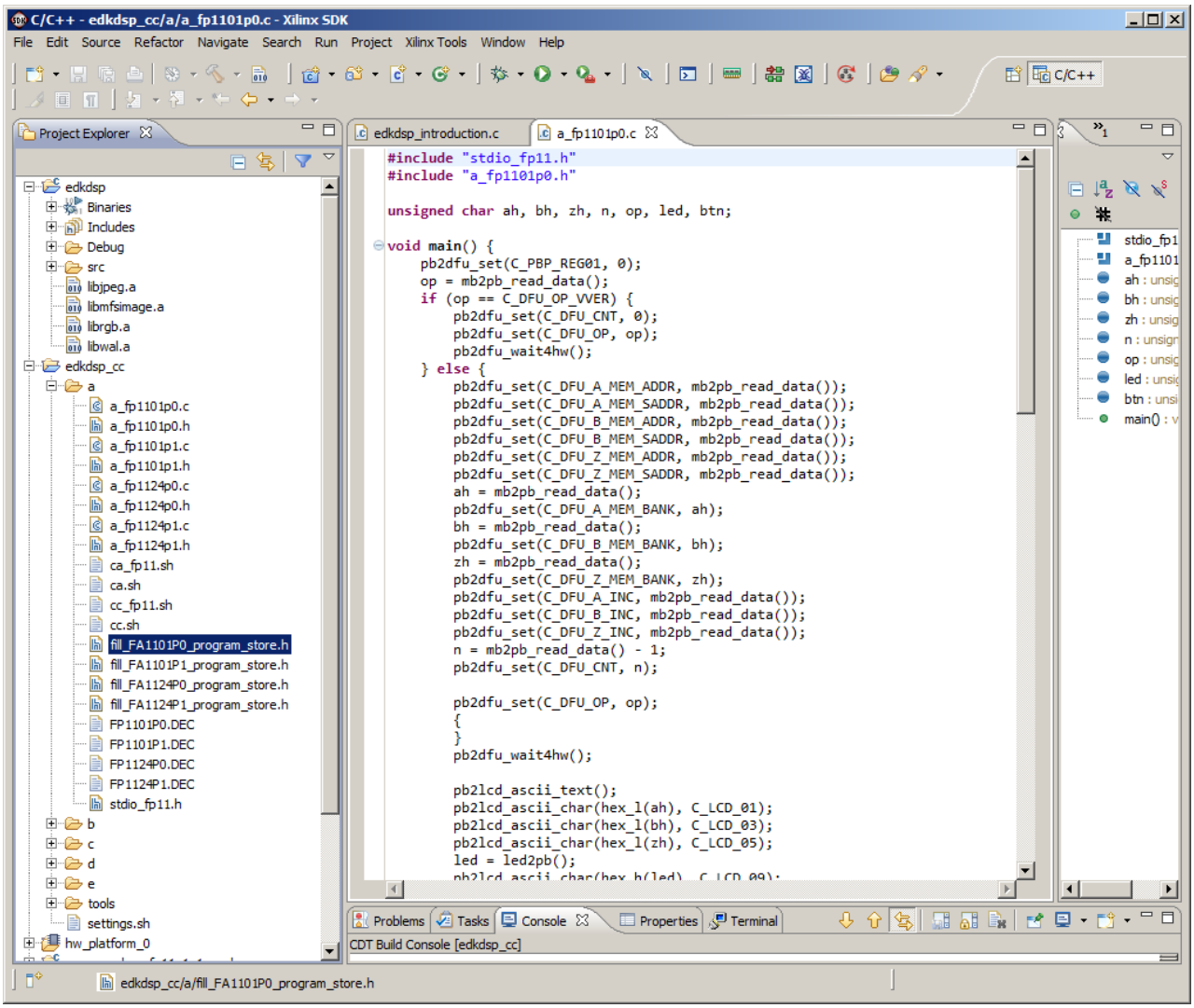

Figure 25: Initial section of the PicoBlaze controller firmware edkdsp_cc\a\a_fp1101p0.c.

Figure 25b presents the final section of the PicoBlaze firmware program edkdsp_cc\a\a_fp1101p0.c .
Before terminating, the PicoBlaze is communicating support information to several ''Screens''. It is using function **pb2mb_write()** to write a single byte to MicroBlaze. Each screan is terminated by function call **pb2mb_eoc()**. This process of data exchange with MicroBlaze is terminated by selecting Screen0. See Figure 26. and the corresponding Figure 24. MicroBlaze prints received data to the console in this simple introduction example.

Larger demo presented on Figure 4 and Figure 5 is presenting execution of the same firmware (See Figure 25 and Figure 26) with output to the XGA display screens and to ascii file FP1101.TXT in the DDR2 RAM-based file system of MicroBlaze processor. The FP1101.TXT file can be uploaded from the DDR2 to the PC by Ethernet with support of TFTP server running on the MicroBlaze processor on the 3S700AN board [6].

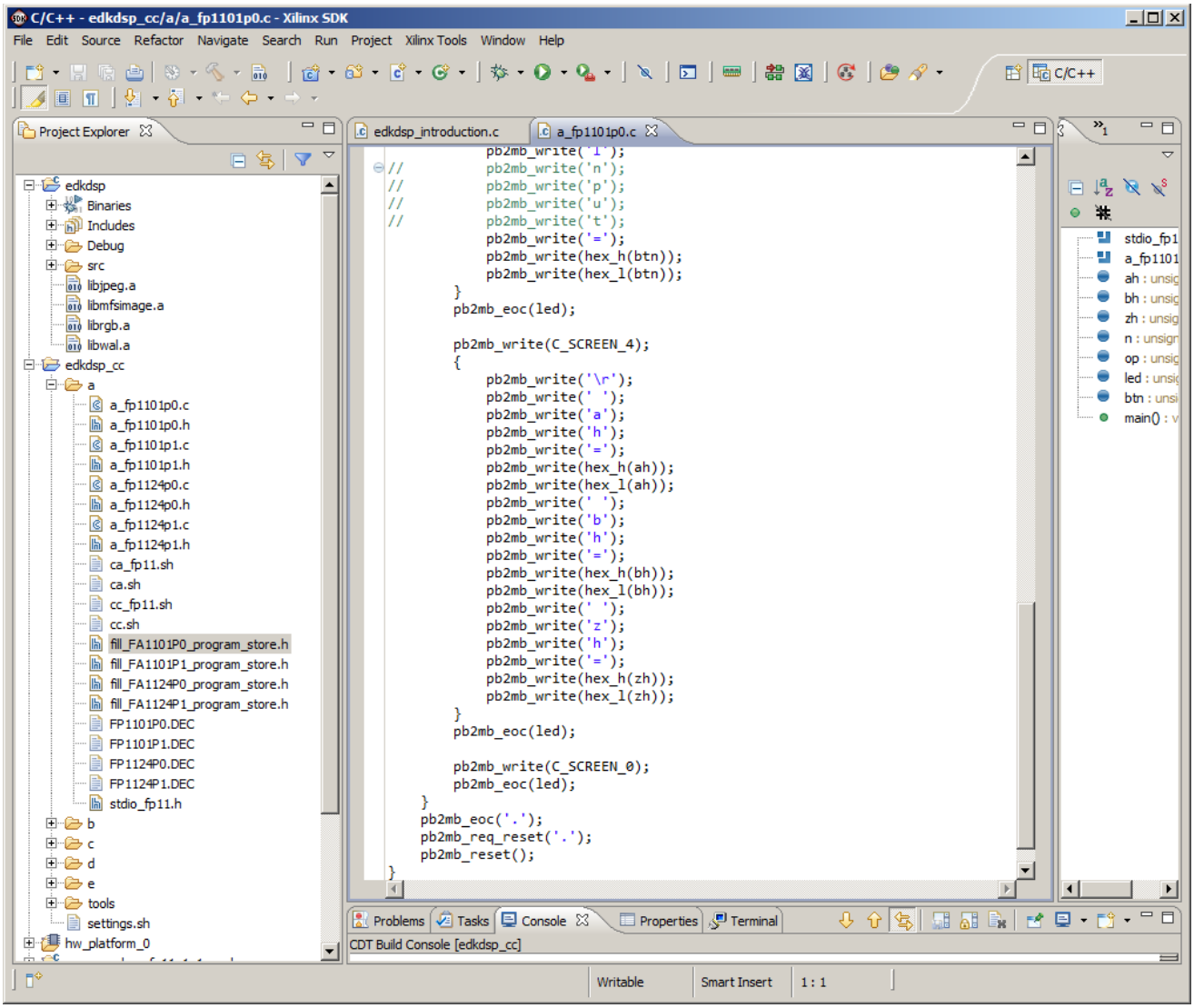

Figure 26: Final section of the PicoBlaze controller firmware edkdsp_cc\a\a_fp1101p0.c.

The PicoBlaze firmware program edkdsp_cc\b\b_fp1101p0.c demonstrates use of user defined function calls. The C function prime() is computing some first prime numbers in PicoBlaze in parallel with the vector floating point computation. See Figure 27. This demo is already precompiled by the EdkDSP C compiler into the header file edkdsp_cc\b\fill_FA1101P0_program_store.h.

In SDK, copy and paste the file fill_ edkdsp_cc/b/FA1101P0_program_store.h into the SDK edkdsp project directory edkdsp\src. In SDK project explorer, select edkdsp project, select ''Clean Project'' to force recompilation the complete MicroBlaze ''edkdsp'' project with new PicoBlaze firmware and test it on the 3S700AN board. Result is displayed on Figure 28.

The PicoBlaze firmware program edkdsp_cc\e\e_fp1101p0.c demonstrates use of 16bit integer variables and computes prime numbers in the (decimal) range <2 … 320>. See Figure 28. Repeat copy and paste, recompile and test on the 3S700AN board. See Figure 30 with the prime numbers computed by the PicoBlaze processor and printed in the hexadecimal format by MicroBlaze.

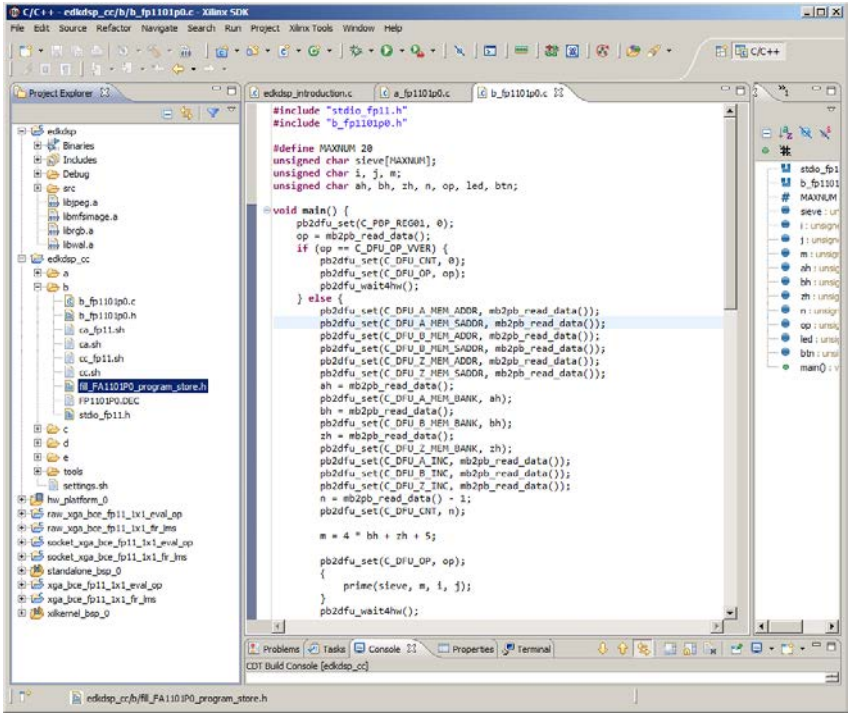

Figure 27: Listing of the PicoBlaze controller firmware program edkdsp_cc\b\b_fp1101p0.c.

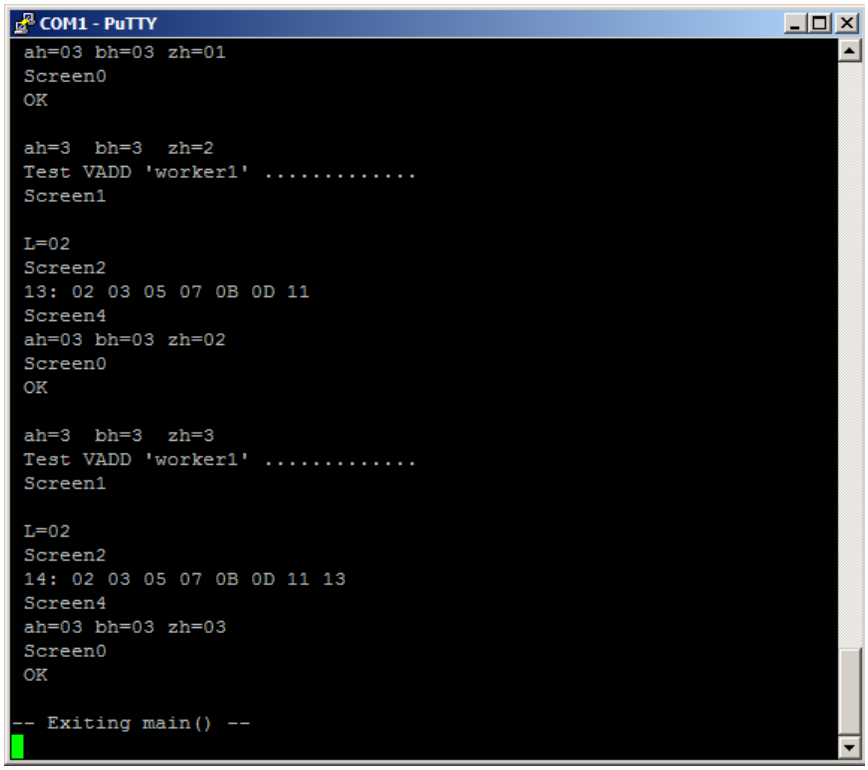

Figure 28: Result of PicoBlaze controller firmware program edkdsp_cc\b\b_fp1101p0.c.

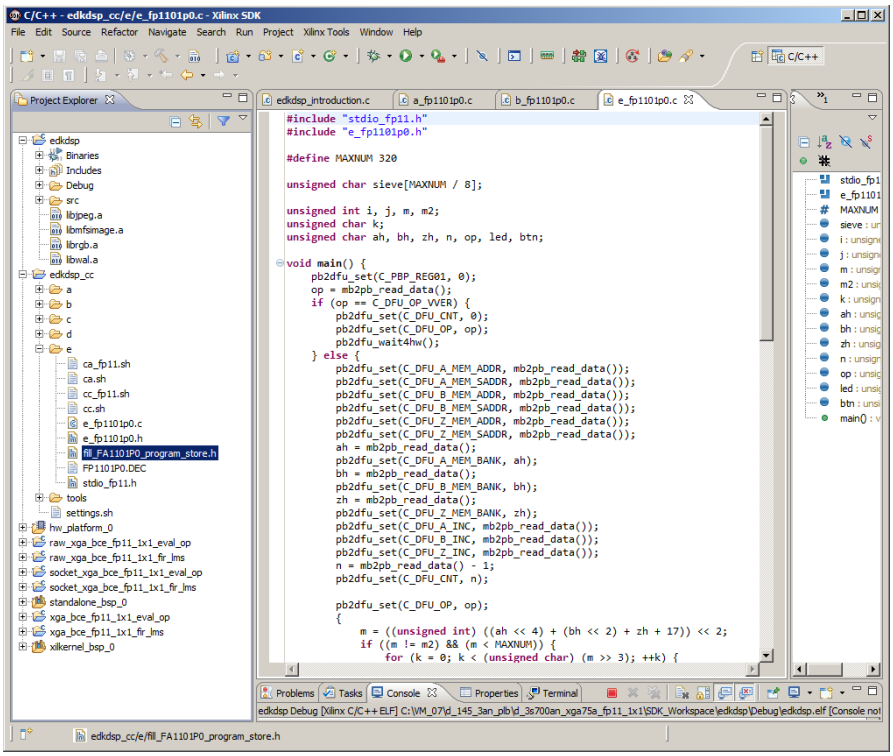

Figure 29:Listing of the PicoBlaze controller firmware program edkdsp_cc\e\e_fp1101p0.c.

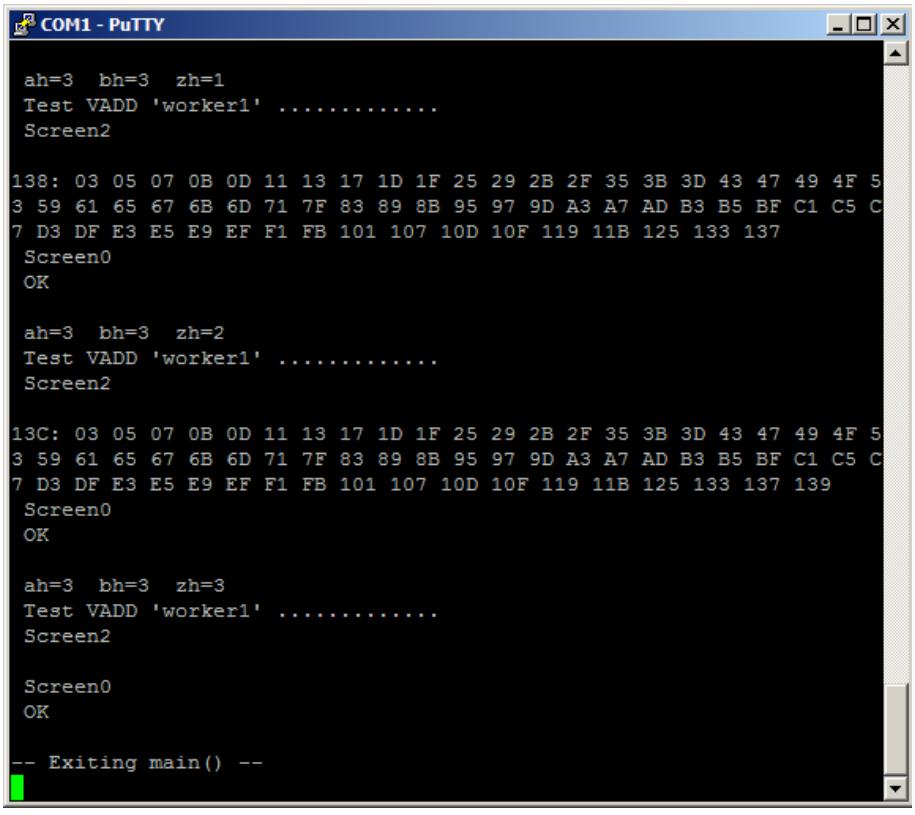

Figure 30: Result of the PicoBlaze controller firmware program edkdsp_cc\e\e_fp1101p0.c.

3.3 Evaluation and use of the EdkDSP C compiler

This section describes the use of the EdkDSP C compiler to recompile the firmware for the PicoBlaze controller of EdkDSP accelerators. The evaluation package includes also precompiled files with the firmware ready for download from PC to the 3S700AN board. These files can be used if the EdkDSP C compiler is not installed on your PC. The UTIA EdkDSP C compiler is implemented as Ubuntu binary utility.

An "VMware player" software and a compatible Ubuntu image version is needed to run the UTIA EdkDSP C compiler on Windows 7 (64bit or 32bit) PC. The Ubuntu image used in UTIA needs two DVD disks (8GB). That is why it is not included as part of the evaluation package.

If you would need this image, write an email request to kadlec@utia.cas.cz to get these two DVD with correct Ubuntu image from UTIA (free of charge) by standard mail.

Install from the Internet the VMware Player software (64bit or 32bit) on your PC. Open the VMware Player and select the "Ubuntu_EdkDSP" image.
The Ubuntu will start. Login as:
User: devel
Pswd: devuser

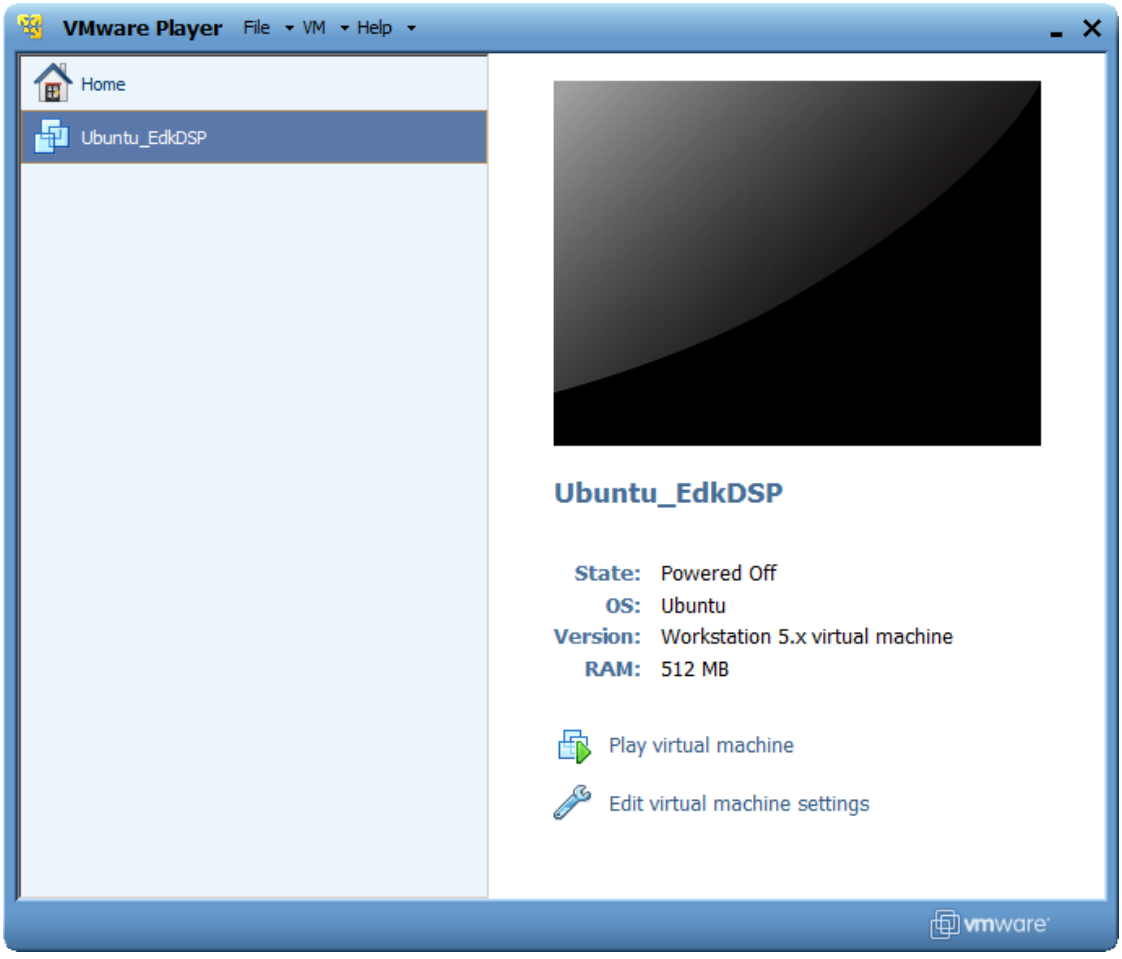

Figure 31: Select the Ubuntu_EdkDSP image in the VMware Player and click "Play Virtual machine".

The VMware Player creates virtual Ethernet connections to the PC.
The PC directory c:\VM_07 needs to be shared by Windows 7 and the Ubuntu applications by Samba.

In Windows 7, set the directory c:\VM_07 as the shared directory.
In Ubuntu, open terminal and mount the PC directory c:\VM_07 to Ubuntu by Samba.

This has been done by the script samba_07.sh. Script is asking for the Ubuntu user password and your Password in Windows 7.

The Windows 7 c:/VM_07 directory is mounted to the Ubuntu OS as:
/mnt/cdrive

In Ubuntu, change directory to:
/mnt/cdrive/d_145_3an_plb/d_3s700an_xga_75a_fp12_1x1/SDK_Workspace/edkdsp_cc
The EdkDSP C compiler utilities have to be on the Ubuntu PATH. This is done by sourcing the settings.sh script in this directory. Type:
source settings.sh
The EdkDSP C compiler utilities located in the directory
c:/VM/d_145_3an_plb/d_3s700an_xga75a_fp11_1x1/edkdsp_cc/tools/linux-i386/utia/bin/
are on the PATH path. See Figure 32.
In Ubuntu, change directory to the example directory : ./a

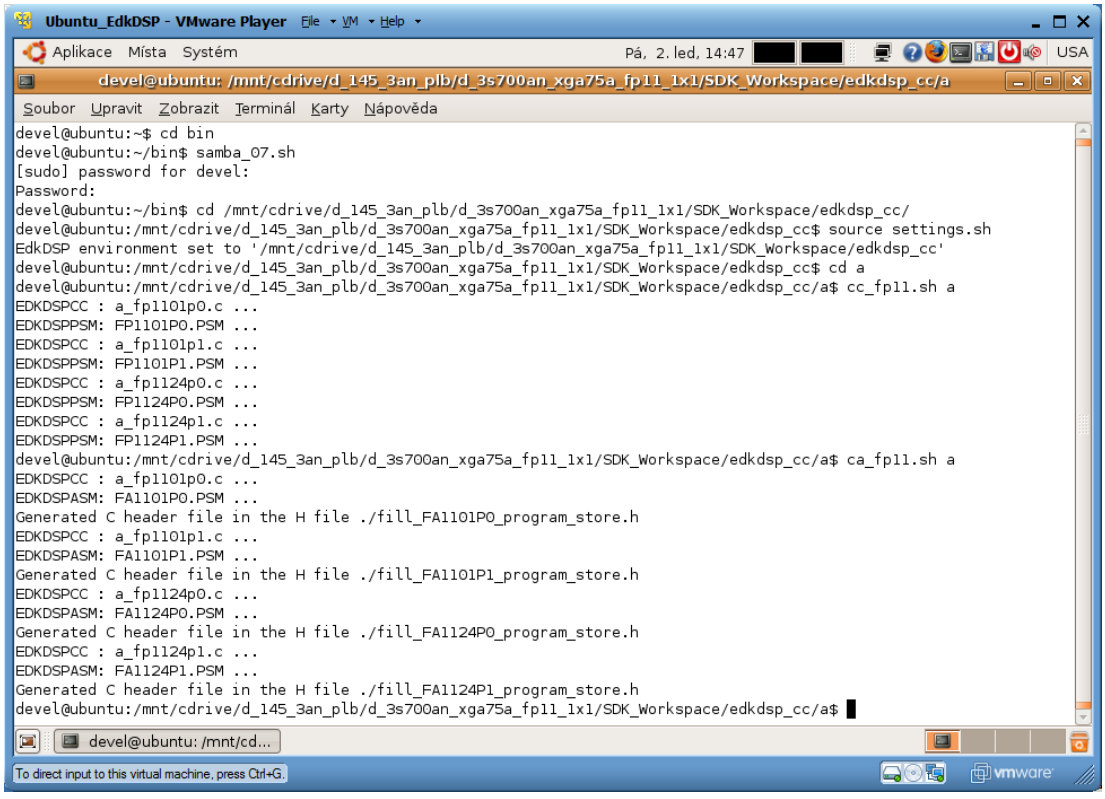

Figure 32: Set samba to the directory shared with Win7, source settings.sh script to set the PATH to the EdkDSP C compiler binary utilities, change directory and compile the firmware

C examples can be compiled by script script cc_fp11.sh with parameter a. Type:
cc_fp11.sh a

This script will recompile and assemble all four C programs present in this directory into .DEC files, ready for download by the Windows 7 TFTP client to the ram-based file system of the 3S700AN board. See Figure 31.

C examples can be also compiled by the script ca_fp11.sh with parameter a. Type:
ca_fp11.sh a

This script will recompile and assemble all four C programs into .h C header files and .m Matlab scripts. The header files can be used to modify the default PicoBlaze firmware headers (included in the MicroBlaze source code) without need of the TFTP download of .DEC files via Ethernet. See Figure 31.

Example of use of header files: In SDK, you can copy and paste the generated fill_FA1101P0_program_store.h and fill_FA1101P0_program._store.h files into the SDK edkdsp project directory edkdsp\src, recompile the edkdsp project and test it on board with new firmware, without the TFTP support.

3.4 Examples of firmware modifications

Use of EdkDSP C compiler will be presented in this section. We will change, recompile and execute the PicoBlaze firmware program edkdsp_cc\a\a_fp1101p0.c. See Figure 25b for the original code and Figure 33 for the modified code. Instead of printing the accelerator external input as I= we will print from PicoBlaze to the MicroBlaze Input=. See Figure 33

The modified firmware edkdsp_cc/a/a_fp1101p0.c is recompiled as indicated in Figure 34. In SDK, copy and paste the generated fill_FA1101P0_program_store.h and fill_FA1101P1_program_store.h files into the SDK edkdsp project directory edkdsp/src, recompile the edkdsp project and test it on board with new firmware.

Result is displayed on Figure 35. Please compare it with Screen3 string I= has been replaced with the string Input= as expected.

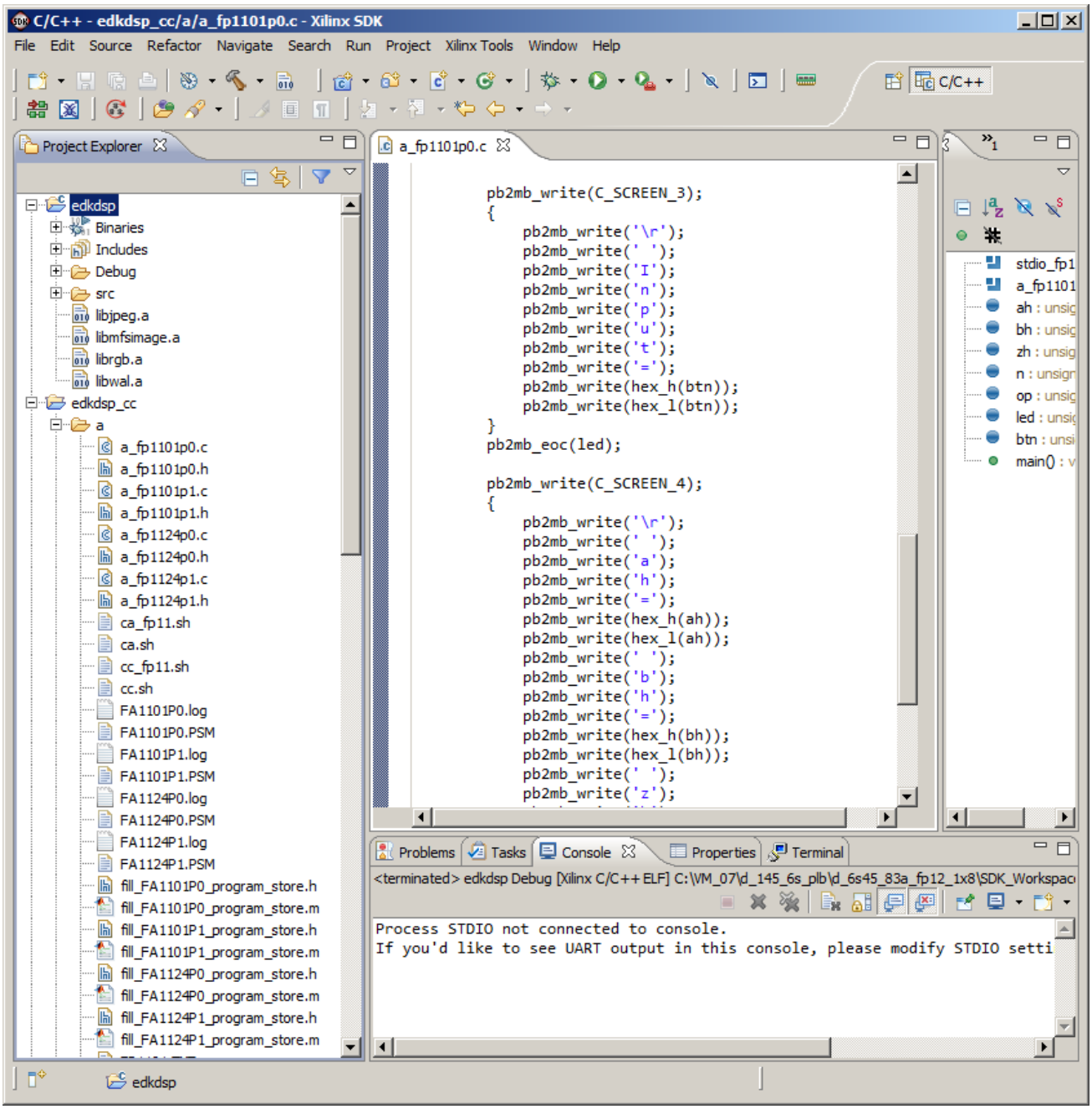

Figure 33: Example of simple modification of edkdsp_cc\a\a_fp1101p0.c ('I=' is changed to 'Input=')

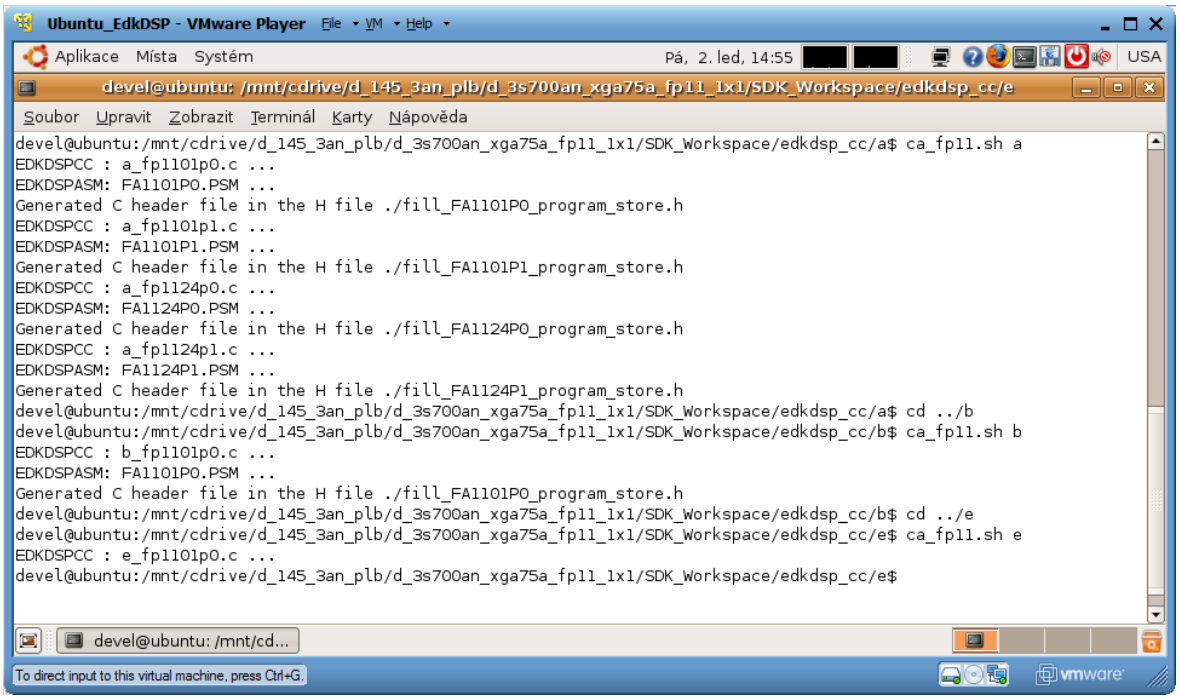

Figure 34: EdkDSP compilation of the modified edkdsp_cc/a/a_fp1101p0.c code in Ubuntu

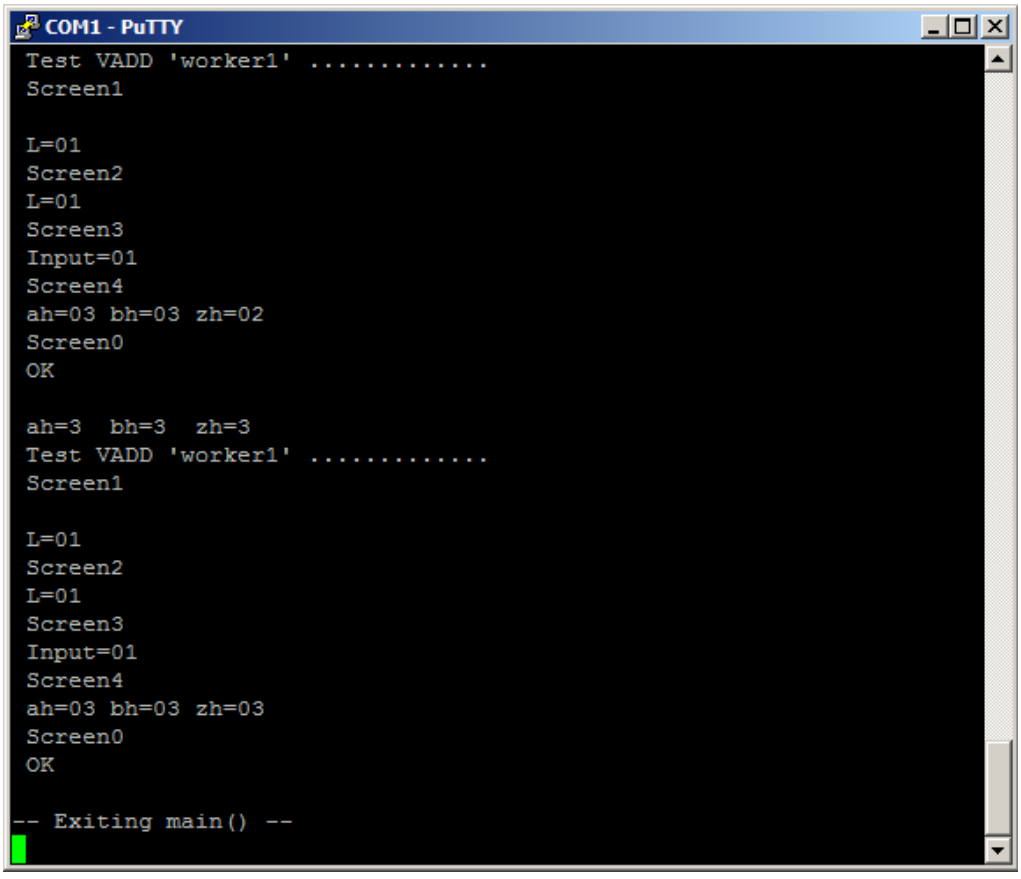

Figure 35: Result of PicoBlaze controller program a_fp110p0.c with 'I=' replaced by 'Input='

3.5 Compilation of all PicoBlaze exampes

Compilation of edkdsp_cc/b/b_fp110p0.c … edkdsp_cc/e/e_fp110p0.c demos is similar.
In Ubuntu, change the directory and recompile by included scripts. Example:

```
cd ../b
cc_fp11.sh b
ca_fp11.sh b
…
cd ../e
cc_fp11.sh e
ca_fp11.sh e
```

The firmware edkdsp_cc\b\b_fp110p0.c computes prime numbers in the range from 2 to 20.
It is computed in parallel with the vector floating point computation pf the 8xSIMD data flow unit. See Figure 32.
It documents the use of user defined functions, declaration and use of single dimensional array in the EdkDSP C compiler for the PicoBlaze controller.

Compilation can be seen on Figure 34. Listing of the firmware edkdsp_cc\b\b_fp110p0.c is presented in Figure 27. Results printed on the console are displayed on Figure 28.

Firmware edkdsp_cc\c\c_fp110p0.c perform identical computation of prime numbers as b_fp110p0.c.
It is documenting effects of the declaration of C variables dynamically in stack instead of the declaration as global variables.

Firmware edkdsp_cc\d\d_fp110p0.c directory is computing prime numbers in the range from 2 to 255. This C code is documenting the access to bits in an unsigned char array and the use of the unsigned int data type (with 16 bit values).

Firmware edkdsp_cc\e\e_fp110p0.c directory is computing prime numbers in the range from 2 to 320. The algorithm is documenting printing and display of data larger than 0xFF. Compilation can be seen on Figure 34. Listing of the firmware edkdsp_cc\e\e_fp110p0.c is presented in Figure 29. Results printed on the console are displayed on Figure 30.

Detailed information about PicoBlaze based peripheral controllers, related designs and the ASM language programming of the PicoBlaze processor can be found in Xilinx application notes and design examples [12], [13], [14], [15] designed and supported by Ken Chapman and also in the designs and application notes from project VLAM [16], [17] (in Czech language).

3.6 EdkDSP C compiler parameters, restrictions and the EdkDSP PicoBlaze API

The EdkDSP C compiler supports these data types:

- unsigned char 8 bit values 0x0 ... 0xFF
- char 8 bit values 0x80 ... 0x7F
- unsigned int 8 bit values 0x0 ... 0xFFFF
- int 16 bit values 0x8000 ... 0x7FFF
- Single dimensional array of unsigned char, char, unsigned int or int elements is supported.
- Pointer type pointing to the array, pointing to the array element or to the variable is supported.
- Function calls with all supported data types or pointers to these data types as output and input arguments.

Restrictions of the EdkDSP C compiler.

- 32 bit integer (signed or unsigned) data type is not supported.
- Array of pointers is not supported.
- Structures are not supported.
- Global variables and arrays can be only declared. They are NOT initialised to zero and cannot be statically initialised by the compiler. Content of global variables must be defined in the program.
- Text strings are not supported.

Restriction related to size of the PicoBlaze controller:

The PicoBlaze is working with only 64 bytes of the internal scratch pad memory. This memory serves for all C program variables and arrays and it is also used by the C program stack.
Program size is limited to max 1024 assembly code instructions. Each instruction is 18 bit wide.
All assembler instructions are executed in 2 clock cycles.

Programming guidelines related to the restriction of the EdkDSP C compiler.

Use of Global variables and arrays if possible. It results in faster code.
Use software initialisation of Global variables and arrays as the first step of your program.

If two subsequent C programs use an identical set of global variables and arrays, the variables will be allocated in identical locations of the scratch pad memory. If the first program performs software initialisation of global variables and arrays, performs some computations and terminates, the second program can take the advantage of initialised global variables left from the first program in the scratch pad memory. The sequence of declaration of global variables, data types and the size of arrays must be identical to make this method valid.

Optimisations performed by EdkDSP C compiler:

Expressions with constants known in the compile time are computed by the compiler and only the resulting constant is entering into the compilation process.
The compiler is using fixed set of processor registers for transfer of parameters and results in function calls. This helps to work with mixed C and ASM language programming. The PicoBlaze I/O functions
are defined in the ASM language and declared as functions callable from C code.
The reserved PicoBlaze registers (unused by the EdkDSP C compiler) can be used by the ASM language code functions. This is possible only if the interrupt is not used and if the ASM language code functions do not call another ASM language code functions.

EdkDSP C PicoBlaze programs can use this I/O API functions optimised in the ASM:

unsigned char mb2pb_read_data();	Read value from MicroBlaze (blocking, includes handshake with MicroBlaze SW)
void pb2mb_write(unsigned char data);	Write data value from PicoBlaze to MicroBlaze (blocking, includes handshake with MicroBlaze SW)
void pb2mb_eoc(unsigned char data);	Write data value from PicoBlaze to MicroBlaze and indicate the end of string flag (blocking, includes handshake with MicroBlaze SW)
void pb2mb_req_reset(unsigned char data);	Write data value from PicoBlaze to MicroBlaze and indicate request from to reset PicoBlaze (blocking, includes handshake with MicroBlaze SW)
void pb2mb_reset();	Activate PicoBlaze reset from PicoBlaze program with MicroBlaze support (blocking, includes handshake with MicroBlaze SW)
unsigned char led2pb();	Read PicoBlaze LED port
unsigned char btn2pb();	Read PicoBlaze BTN port
unsigned char hex_h(unsigned char ch);	Write hexadecimal ascii representation of the high 4bit of the input 8bit argument from PicoBlaze to MicroBlaze (blocking, includes handshake with MicroBlaze SW)
unsigned char hex_l(unsigned char ch);	Write hexadecimal ascii representation of the low 4bit of the input 8bit argument from PicoBlaze to MicroBlaze (blocking, includes handshake with MicroBlaze SW)
void pb2dfu_set(unsigned char mem, unsigned char data);	Write 8bit data to the PicoBlaze I/O port mem
void pb2dfu_wait4hw();	Wait for the end of the EdkDSP floating point, vector operation (blocking, waits for the end of the FP vector operation)
void pb2lcd_ascii_char(unsigned char ch, unsigned char pos);	Write to local 2x16 lcd display. (In case of no HW support, the function will write to unconnected ports with no effect).

User can call these optimized ASM functions from C.
User can define own C functions or ASM functions and include them in .h file or directly in the C code.

User defined functions can be defined and tested in C code first. The compiled ASM code can be often included in the next stage with some additional optimisations leading to shorter code and improved performance.

Examples of this approach to the optimisation can be seen in the included EdkDSP C source code examples edkdsp_cc\a … edkdsp_cc\e.

3.7 Short overview of all SW projects included in the package.

This application note presents source code of several projects working with the EdkDSP accelerator. The package includes several modifications of these projects:

- SDK SW projects with “xga” in the name are supporting RGB display with resolution 1024x768p70 and rgb444 pixels. These projects have no file system support and no Ethernet support. These SW projects can be used without an operating system or used as applications for the Petalinux operating system port (without MMU) for the 3S700AN board.

- SDK SW projects with “socket” in the name use the socket version of the LwIP library [7]. It works on top of the XilKernel multitasking OS. Projects are supporting RGB565 display 1024x768p70 with output resolution reduced to rgb444 pixels, DDR2 based Xilinx RAM file system, TFTP server and HTTP server. See Figure 1, Figure 4 and Figure 6.

- SDK SW projects with “raw” in the name use the raw version of the LwIP library [7]. It works on top of the RAW BSP without multitasking. The request coming from the Ethernet are processed with set of callback functions. Projects are supporting RGB565 display 1024x768p70 with output resolution reduced to rgb444 pixels, DDR2 based Xilinx RAM file system, TFTP server and HTTP server. See Figure 1, Figure 4 and Figure 6.

Use of examples with Ethernet and TFTP support:

Connect the S3700AN board to 10/100 Mbit PC Ethernet port. In case of 1Gb Ethernet port use a switch to auto negotiate the speed to 100Mb. Set the PC Ethernet port to 192.168.8.2. In SDK, download the bitstream and run the application. Open the Internet explorer on your PC and connect to http:/192.168.8.10. Demo GUI will start. Firmware and log files can be downloaded or uploaded with a Win7 TFTP client connected to the 192.168.8.10. port 69. See Figure 1. GUI button start drawing of .jpg logos ENIAC/PANACHE to demonstrate performance of the area optimised minimal MicroBlaze installation. Another GUI button starts demos similar to the “xga” demos and to the simple edkdsp project. All demos use PicoBlaze firmware identical to the edkdsp project. See Figure 4 and Figure 6.

4. References

[1] Xilinx Spartan-3AN FPGA Family Data Sheet, DS557 (v4.2) June 12, 2014, Product Specification.
http://www.xilinx.com/support/documentation/data_sheets/ds557.pdf

[2] Extended Spartan-3A Family Overview, DS706 (v1.1) February 2, 2011, Product Specification
http://www.xilinx.com/support/documentation/data_sheets/ds706.pdf

[3] Spartan-3 Generation FPGA User Guide, Extended Spartan-3A, Spartan-3E, and Spartan-3 FPGA Families UG331 (v1.8) June 13, 2011
http://www.xilinx.com/support/documentation/user_guides/ug331.pdf

[4] Spartan-3 Generation Configuration User Guide, Extended Spartan-3A, Spartan-3E, and Spartan-3 FPGA Families, UG332 (v1.6) October 26, 2009
http://www.xilinx.com/support/documentation/user_guides/ug332.pdf

[5] Spartan-3AN FPGA, In-System Flash, User Guide, For Spartan-3AN FPGA applications that read or write data to or from the In-System Flash memory after configuration UG333 (v2.3) October 16, 2014
http://www.xilinx.com/support/documentation/user_guides/ug333.pdf

[6] Spartan-3A/3AN FPGA Starter Kit Board User Guide UG334 (v1.1) June 19, 2008
http://www.xilinx.com/support/documentation/boards_and_kits/ug334.pdf

[7] Xilinx XAPP1026 (v3.2) October 28, 2012. LightWeight IP (lwIP) Application Examples
Authors: Anirudha Sarangi and Stephen MacMahon
http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf

[8] PANACHE, Pilot line for Advanced Nonvolatile memory technologies for Automotive microControllers, High security applications and general Electronics. Project no: ENIAC JU 621217, MSMT 7H14006
Project coordinator is STMicroelectronics, Crolles, France.
http://sp.utia.cz/index.php?ids=projects/panache

[9] UTIA download page for this application note and free evaluation package ready for download.
Select: EdkDSP Demonstrator in Xilinx 3S700AN FPGA with Embedded FLASH and NV RAM.
http://sp.utia.cz/index.php?ids=results

[10] PicoBlaze 8-bit Embedded Microcontroller User Guide for Extended Spartan 3 and Virtex5 FPGAs; Introducing PicoBlaze for Spartan-6, Virtex-6, and 7 Series FPGAs. UG129 June 22, 2011.
http://www.xilinx.com/support/documentation/ip_documentation/ug129.pdf

[11] MicroBlaze Soft Processor Core, Xilinx.
http://www.xilinx.com/tools/microblaze.htm

[12] Spartan-3E FPGA Starter Kit Board Design Examples, Xilinx
http://www.xilinx.com/products/boards/s3estarter/reference_designs.htm

[13] Spartan-3A/3AN FPGA Starter Kit Board Design Examples, Xilinx
http://www.xilinx.com/products/boards/s3astarter/reference_designs.htm

[14] Ken Chapman, Initial Design for Spartan-3E Starter Kit (LCD Display Control), Xilinx Ltd, 16.2.2006
http://www.xilinx.com/products/boards/s3estarter/files/s3esk_startup.pdf

[15] Ken Chapman, Rotary Encoder Interface for Spartan-3E Starter Kit, Xilinx Ltd, 20.2.2006
http://www.xilinx.com/products/boards/s3estarter/files/s3esk_rotary_encoder_interface.pdf

[16] Peripheral Controllers for Spartan3E Starter Kit Development Board, UTIA, evaluation package, XPD 9.2 projects, PicoBlaze, Spartan3E, evaluation designs and application notes (in Czech).
http://sp.utia.cz/index.php?ids=results&id=s3eperip&lang=eng

[17] VLAM, Virtual Laboratory of Microprocessor Technology Applications, Project No.: 2C06008, NPV2-Information Society program, Ministry of Education, Youth and Sports of the Czech Republic, PicoBlaze, Spartan3E, evaluation designs and application notes (in Czech).
http://sp.utia.cz/index.php?ids=projects/vlam

5. Deliverables for the evaluation version of EdkDSP 3S700AN.

The enclosed **Evaluation version of the EdkDSP demonstrator for 3S700AN package** of can be downloaded from UTIA www page [9] free of charge and used for evaluation of EdkDSP accelerators on Windows 7 (32 or 64 bit).

The evaluation package includes (on 1 DVD) or as www download package these deliverables:

12 precompiled designs with UTIA EdkDSP accelerators for Xilinx 3S700AN board, compiled in Xilinx EDK 14.5 and XPS (ISE) 14.5. The UTIA EdkDSP accelerators are compiled with HW limit on number of vector operations. The termination of the evaluation license is reported in advance by the demonstrator on the terminal as well as on the display.

The evaluation package includes SDK 14.5 SW projects in source code for MicroBlaze. Projects support the family of UTIA EdkDSP accelerators for Xilinx 3S700AN board.

The evaluation package includes these libraries:

libwal.a	EdkDSP api (SDK 14.5, MicroBlaze) for EdkDSP accelerators, 3S700AN, PLB.
librgb.a	EdkDSP api (SDK 14.5, MicroBlaze) for Xilinx PLB display controller.
libjpeg.a	EdkDSP api (SDK 14.5, MicroBlaze) for decompression of .jpg pictures.
libmfsimage.a	EdkDSP filesystem Image in form of a library. (It can be linked to the MicroBlaze .elf).

These libraries have no time restriction. The evaluation license is provided by UTIA only for the use with the family of UTIA EdkDSP accelerators designed for the Xilinx 3S700AN board. Source code of these libraries is owned by UTIA and it is not provided in this evaluation package.

The evaluation package includes these binary applications for Ubuntu:

edkdsppp	EdkDSP C pre-processor binary for Ubuntu (x86 PC) under the VMware Player.
edkdspcc	EdkDSP C compiler binary for Ubuntu (x86 PC) under the VMware Player.
edkdsppsm	EdkDSP ASM compiler binary for Ubuntu (x86 PC) under the VMware Player.
edkdspasm	EdkDSP ASM compiler binary for Ubuntu (x86 PC) under the VMware Player.

These binary applications have no time restriction. The user of the evaluation package has license from UTIA to use these utilities for compilation of the firmware for the Xilinx PicoBlaze processor inside of the UTIA EdkDSP accelerators in the 12 precompiled designs for the Xilinx 3S700AN board with PLB bus. The source code of these applications is owned by UTIA and it is not provided in the evaluation package.

The evaluation package includes demonstration firmware in C source code for the Xilinx PicoBlaze processor in the family of UTIA EdkDSP accelerators for the Xilinx 3S700AN board.

The evaluation package also includes compiled versions of this firmware. The compiled firmware files can be downloaded into the UTIA EdkDSP accelerators for the Xilinx 3S700AN board without the need to install of the Ubuntu (x86 PC) image under the VMware Player.

On email request to kadlec@utia.cas.cz , UTIA will send 2 DVD CDs (8GB) with the Ubuntu (x86 PC) image for the VMware Player free of charge.

6. Deliverables for the EdkDSP 3S700AN demonstrator for PANACHE project partners

The EdkDSP demonstrator for the 3S700AN for PANACHE project partners can be ordered from UTIA AV CR, v.v.i., by email request for quotation to kadlec@utia.cas.cz. UTIA will provide quotation by email. After the confirmed order (based on the UTIA AV CR, v.v.i., email quotation) received by email to kadlec@utia.cas.cz. UTIA AV CR, v.v.i. will deliver (by standard mail) to the customer the printed version of this application note together with 3 DVDs with deliverables described in this section. UTIA AV CR, v.v.i., will send to the customer (by email) and by the standard mail the invoice for:

Release version of the EdkDSP demonstrator for 3S700AN
for PANACHE project partners (without VAT) **0,00 Eur**

The package includes this application note and the EdkDSP DVD with these deliverables:

12 precompiled designs with UTIA EdkDSP accelerators for Xilinx 3S700AN board, compiled in Xilinx EDK 14.5 and XPS (ISE) 14.5. The UTIA EdkDSP accelerators included in these designs are compiled with **HW limit on number of vector operations.**

The demonstrator for PANACHE project partners includes source code of all 12 EDK design projects with UTIA EdkDSP accelerators provided as these PLB netlist pcores generated in Xilinx ISE 14.5:

bce_fp11_1x1_0_plbw_v1_10_a	ADD,SUB,MUL
bce_fp11_1x1_0_plbw_v1_11_a	ADD,SUB,MUL,ROTARY
bce_fp11_1x1_0_plbw_v1_12_a	ADD,SUB,MUL,LCD
bce_fp11_1x1_0_plbw_v1_13_a	ADD,SUB,MUL,ROTARY,LCD
bce_fp11_1x1_0_plbw_v1_20_a	ADD,SUB,MUL,MAC
bce_fp11_1x1_0_plbw_v1_21_a	ADD,SUB,MUL,MAC,ROTARY
bce_fp11_1x1_0_plbw_v1_22_a	ADD,SUB,MUL,MAC,LCD
bce_fp11_1x1_0_plbw_v1_23_a	ADD,SUB,MUL,MAC,ROTARY,LCD
bce_fp11_1x1_0_plbw_v1_30_a	ADD,SUB,MUL,MAC,PROD
bce_fp11_1x1_0_plbw_v1_31_a	ADD,SUB,MUL,MAC,PROD,ROTARY
bce_fp11_1x1_0_plbw_v1_32_a	ADD,SUB,MUL,MAC,PROD,LCD
bce_fp11_1x1_0_plbw_v1_33_a	ADD,SUB,MUL,MAC,PROD,ROTARY,LCD
basic_io_core.ngc	Rotary encoder controller with fixed PicoBlaze NV RAM firmware
upb_master.ngc	General I/O controller with fixed PicoBlaze NV RAM firmware
lcd_core.ngc	LCD controller with fixed PicoBlaze NV RAM firmware

These UTIA EdkDSP evaluation netlist pcores for PANACHE project partners **have HW limit on number of vector operations.** The user of the release package has license from UTIA to integrate these netlists into its own ISE 14.5 designs and to compile them to unlimited number of bit-streams for the Xilinx Spartan FPGA designs with the MicroBlaze and the PLB bus. The source code of the EdkDSP accelerators is IP owned by UTIA and it is not provided in the release package to the user.

The package includes SDK 14.5 SW projects in source code for MicroBlaze as described in this application note. Projects support the family of UTIA EdkDSP accelerators for Xilinx 3S700AN board.
The release package includes these libraries:

libwal.a	EdkDSP api (SDK 14.5, MicroBlaze) for EdkDSP accelerators, 3S700AN, PLB.
librgb.a	EdkDSP api (SDK 14.5, MicroBlaze) for Xilinx PLB display controller.
libjpeg.a	EdkDSP api (SDK 14.5, MicroBlaze) for decompression of .jpg pictures.

These libraries have no time restriction. User has license from UTIA for linking of these libraries to MicroBlaze applications with UTIA EdkDSP accelerators for 3S700AN, PLB bus. The source code of these libraries is owned by UTIA and it is not provided in the release package.

The package includes library:

mfsimage	EdkDSP filesystem Image in form of a library. (It can be linked to the MicroBlaze .elf).

Source code for generation of the **libmfsimage.a** by the user is included in the release package.

The package includes these binary applications:

edkdsppp	EdkDSP C pre-processor binary for Ubuntu (x86 PC) under the VMware Player.
edkdspcc	EdkDSP C compiler binary for Ubuntu (x86 PC) under the VMware Player.
edkdsppsm	EdkDSP ASM compiler binary for Ubuntu (x86 PC) under the VMware Player.
edkdspasm	EdkDSP ASM compiler binary for Ubuntu (x86 PC) under the VMware Player.

These binary applications have no time restriction, and the user of the release package has license from UTIA to use these utilities for compilation of the firmware for the Xilinx PicoBlaze processor inside of the UTIA EdkDSP accelerators provided by the release package for the Xilinx 3S700AN board with PLB bus. The source code of these applications is owned by UTIA and it is not provided in the release package.

The package includes demonstration firmware in C source code for the Xilinx PicoBlaze processor in the family of UTIA EdkDSP accelerators for the Xilinx 3S700AN board. The evaluation package also includes compiled versions of this firmware. The compiled firmware files can be downloaded into the UTIA EdkDSP accelerators for the Xilinx 3S700AN board designs with PLB bus, without the need to install of the Ubuntu (x86 PC) image under the VMware Player.

The package deliverables also includes two DVDs with the Ubuntu (x86 PC) image for the VMware Player (free of charge). This image is provided to ease the installation of the UTIA EdkDSP C compiler on Windows 7 (32bit or 64bit) in the VMware Player.

Any and all legal disputes that may arise from or in connection with the use, intended use of or license for the software provided hereunder shall be exclusively resolved under the regional jurisdiction relevant for UTIA AV CR, v. v. i. and shall be governed by the law of the Czech Republic.

7. Deliverables for the release version of EdkDSP 3S700AN, PLB.

The **release version of the EdkDSP demonstrator for 3S700AN, PLB package** can be ordered from UTIA AV CR, v.v.i., by email request for quotation to kadlec@utia.cas.cz. UTIA will provide quotation by email. After the confirmed order (based on the UTIA AV CR, v.v.i., email quotation) received by email to kadlec@utia.cas.cz. UTIA AV CR, v.v.i. will deliver (by standard mail) to the customer the printed version of this application note together with 3 DVDs with deliverables described in this section. UTIA AV CR, v.v.i., will send to the customer (by email) and by the standard mail the invoice for:

Release version of the EdkDSP demonstrator for 3S700AN, PLB package (without VAT) 400,00 Eur

The release package includes this application note and the EdkDSP DVD with these deliverables:

12 precompiled designs with UTIA EdkDSP accelerators for Xilinx 3S700AN board, compiled in Xilinx EDK 14.5 and XPS (ISE) 14.5. The UTIA EdkDSP accelerators included in these designs are compiled with **no HW limit on number of vector operations.** Therefore, all these precompiled designs of the release package run on 3S700AN without limitations of the evaluation package.

The release package includes source code of all 12 EDK design projects with UTIA EdkDSP accelerators provided as these PLB netlist pcores generated in Xilinx ISE 14.5:

bce_fp11_1x1_0_plbw_v1_10_a	ADD,SUB,MUL
bce_fp11_1x1_0_plbw_v1_11_a	ADD,SUB,MUL,ROTARY
bce_fp11_1x1_0_plbw_v1_12_a	ADD,SUB,MUL,LCD
bce_fp11_1x1_0_plbw_v1_13_a	ADD,SUB,MUL,ROTARY,LCD
bce_fp11_1x1_0_plbw_v1_20_a	ADD,SUB,MUL,MAC
bce_fp11_1x1_0_plbw_v1_21_a	ADD,SUB,MUL,MAC,ROTARY
bce_fp11_1x1_0_plbw_v1_22_a	ADD,SUB,MUL,MAC,LCD
bce_fp11_1x1_0_plbw_v1_23_a	ADD,SUB,MUL,MAC,ROTARY,LCD
bce_fp11_1x1_0_plbw_v1_30_a	ADD,SUB,MUL,MAC,PROD
bce_fp11_1x1_0_plbw_v1_31_a	ADD,SUB,MUL,MAC,PROD,ROTARY
bce_fp11_1x1_0_plbw_v1_32_a	ADD,SUB,MUL,MAC,PROD,LCD
bce_fp11_1x1_0_plbw_v1_33_a	ADD,SUB,MUL,MAC,PROD,ROTARY,LCD
basic_io_core.ngc	Rotary encoder controller with fixed PicoBlaze NV RAM firmware
upb_master.ngc	General I/O controller with fixed PicoBlaze NV RAM firmware
lcd_core.ngc	LCD controller with fixed PicoBlaze NV RAM firmware

These UTIA EdkDSP PLB netlist pcores have **no HW limit on number of vector operations.** The user of the release package has license from UTIA to integrate these netlists into its own ISE 14.5 designs and to compile them to unlimited number of bit-streams for the Xilinx Spartan FPGA designs with the MicroBlaze and the PLB bus. This license has no time restriction. The source code of the EdkDSP accelerators is IP owned by UTIA and it is not provided in the release package to the user.

The release package includes SDK 14.5 SW projects in source code for MicroBlaze as described in this application note. Projects support the family of UTIA EdkDSP accelerators for Xilinx 3S700AN board.
The release package includes these libraries:

libwal.a	EdkDSP api (SDK 14.5, MicroBlaze) for EdkDSP accelerators, 3S700AN, PLB.
librgb.a	EdkDSP api (SDK 14.5, MicroBlaze) for Xilinx PLB display controller.
libjpeg.a	EdkDSP api (SDK 14.5, MicroBlaze) for decompression of .jpg pictures.

These libraries have no time restriction. User has license from UTIA for linking of these libraries to MicroBlaze applications with UTIA EdkDSP accelerators for 3S700AN, PLB bus. The source code of these libraries is owned by UTIA and it is not provided in the release package.

The release package includes library:

mfsimage	EdkDSP filesystem Image in form of a library. (It can be linked to the MicroBlaze .elf).

Source code for generation of the **libmfsimage.a** by the user is included in the release package.

The release package includes these binary applications:

edkdsppp	EdkDSP C pre-processor binary for Ubuntu (x86 PC) under the VMware Player.
edkdspcc	EdkDSP C compiler binary for Ubuntu (x86 PC) under the VMware Player.
edkdsppsm	EdkDSP ASM compiler binary for Ubuntu (x86 PC) under the VMware Player.
edkdspasm	EdkDSP ASM compiler binary for Ubuntu (x86 PC) under the VMware Player.

These binary applications have no time restriction, and the user of the release package has license from UTIA to use these utilities for compilation of the firmware for the Xilinx PicoBlaze processor inside of the UTIA EdkDSP accelerators provided by the release package for the Xilinx 3S700AN board with PLB bus. The source code of these applications is owned by UTIA and it is not provided in the release package.

The release package includes demonstration firmware in C source code for the Xilinx PicoBlaze processor in the family of UTIA EdkDSP accelerators for the Xilinx 3S700AN board. The release package also includes compiled versions of this firmware. The compiled firmware files can be downloaded into the UTIA EdkDSP accelerators for the Xilinx 3S700AN board designs with PLB bus, without the need to install of the Ubuntu (x86 PC) image under the VMware Player.

The release package deliverables also includes two DVDs with the Ubuntu (x86 PC) image for the VMware Player (free of charge). This image is provided to ease the installation of the UTIA EdkDSP C compiler on Windows 7 (32bit or 64bit) in the VMware Player.

Any and all legal disputes that may arise from or in connection with the use, intended use of or license for the software provided hereunder shall be exclusively resolved under the regional jurisdiction relevant for UTIA AV CR, v. v. i. and shall be governed by the law of the Czech Republic.

Disclaimer

This disclaimer is not a license and does not grant any rights to the materials distributed herewith. Except as otherwise provided in a valid license issued to you by UTIA AV CR v.v.i., and to the maximum extent permitted by applicable law:

(1) THIS APPLICATION NOTE AND RELATED MATERIALS LISTED IN THIS PACKAGE CONTENT ARE MADE AVAILABLE "AS IS" AND WITH ALL FAULTS, AND UTIA AV CR V.V.I. HEREBY DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and
(2) UTIA AV CR v.v.i. shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under or in connection with these materials, including for any direct, or any indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or UTIA AV CR v.v.i. had been advised of the possibility of the same.

Critical Applications:
UTIA AV CR v.v.i. products are not designed or intended to be fail-safe, or for use in any application requiring fail-safe performance, such as life-support or safety devices or systems, Class III medical devices, nuclear facilities, applications related to the deployment of airbags, or any other applications that could lead to death, personal injury, or severe property or environmental damage (individually and collectively, "Critical Applications"). Customer assumes the sole risk and liability of any use of UTIA AV CR v.v.i. products in Critical Applications, subject only to applicable laws and regulations governing limitations on product liability.