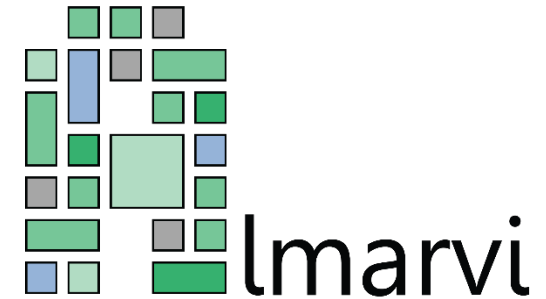


Artemis No. 621439

Algorithms, Design Methods, and Many-Core
Execution Platform for Low-Power Massive Data-
Rate Video and Image Processing



Video Chain Demonstrator on Xilinx Kintex7 FPGA with EdkDSP Floating Point Accelerators

Jiří Kadlec



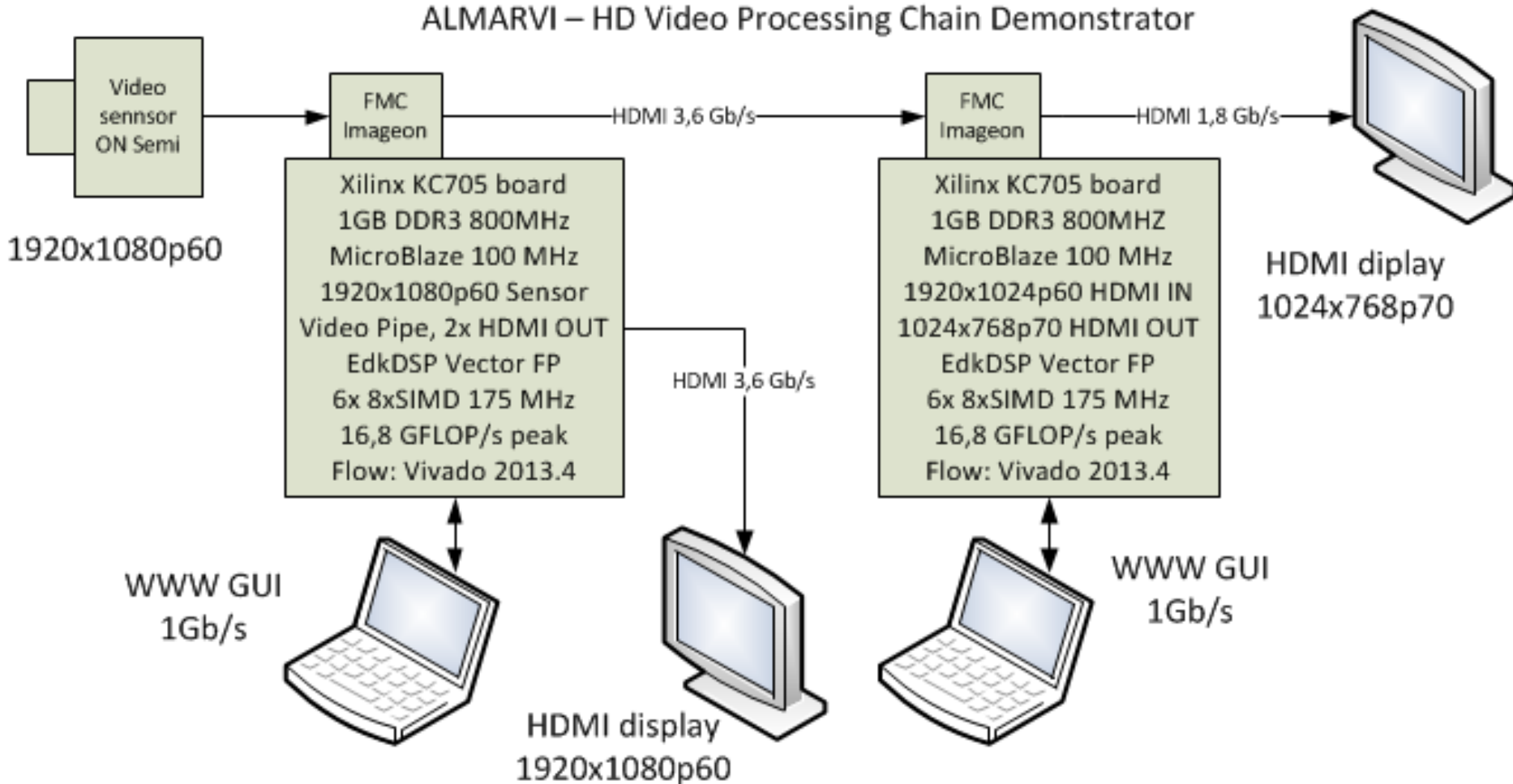
Institute of Information Theory
and Automation of the AS CR



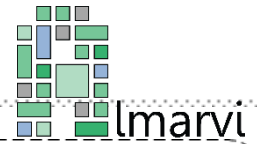
Introduction



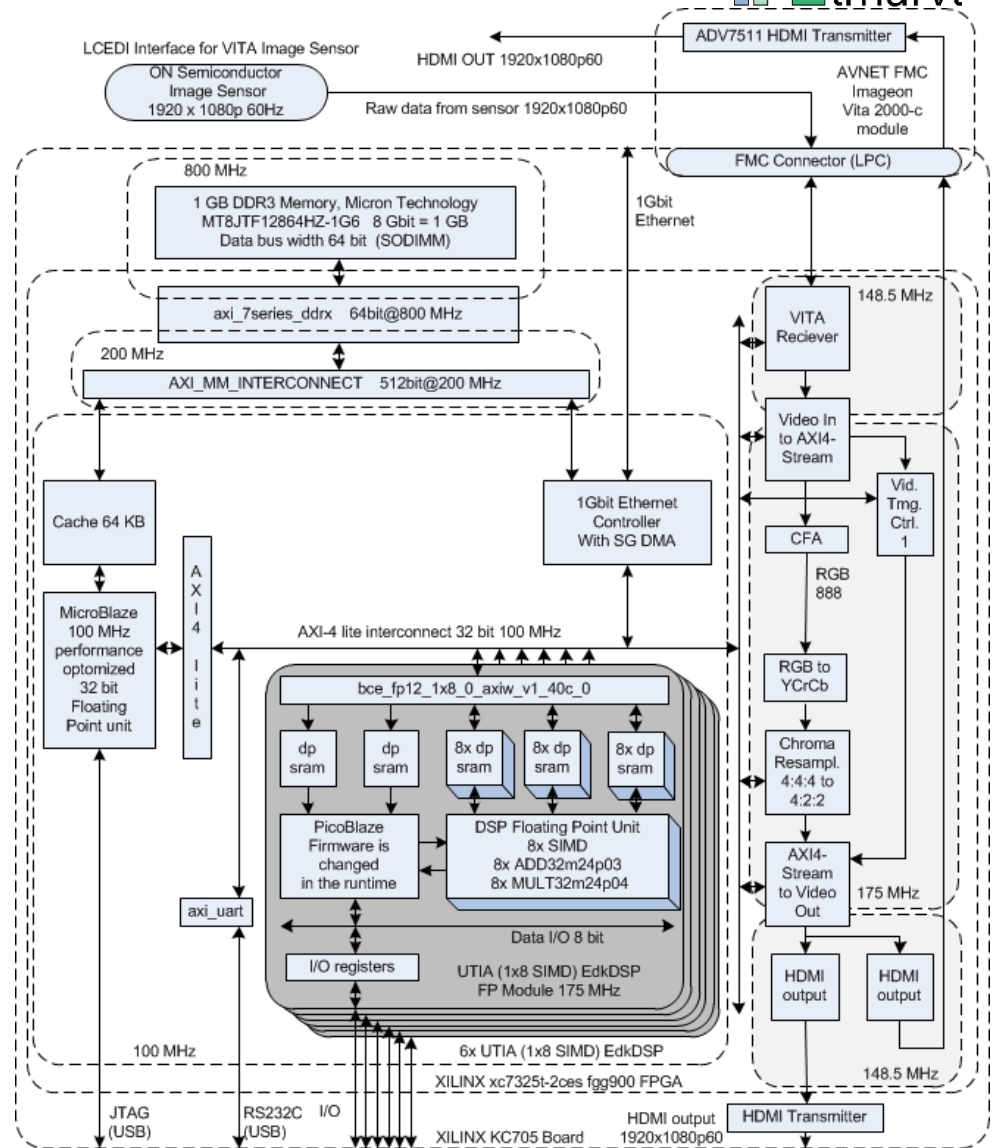
ALMARVI – HD Video Processing Chain Demonstrator



Video Sensor with EdkDSP accelerators



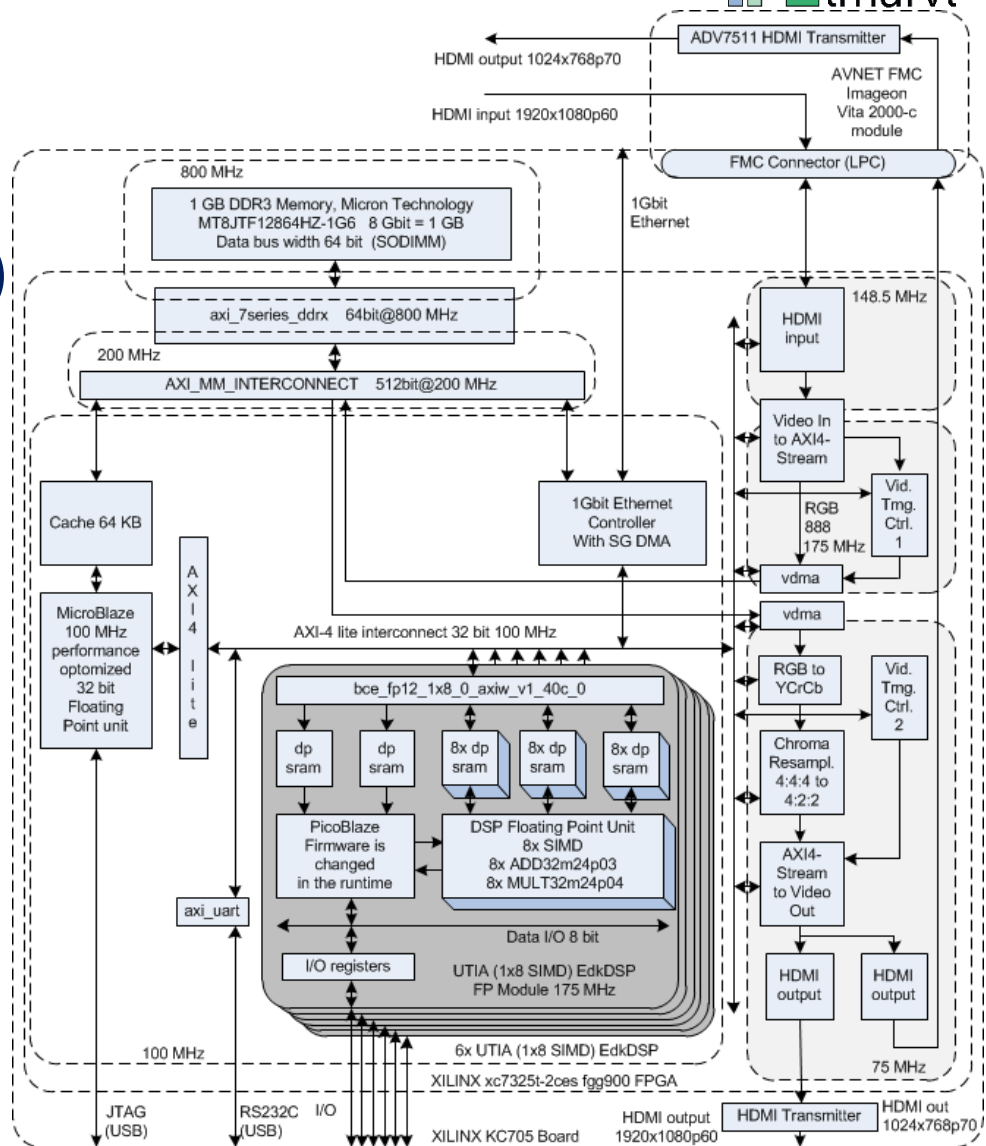
- Xilinx Kintex KC705 board
- ON Semi VITA 2000 color video sensor 1920x1080p60
- HDMI video pass-through
- 6x EdkDSP vector 8xSIMD FP32bit accelerators 175 MHz, peak perf. 16,8 GFLOP
- 6x 8bit PicoBlaze serving as reprogrammable schedulers
- MicroBlaze 32bit 100 MHz
- Xilkernel + LwIP based 1Gb Ethernet Web Server
- 1Gb Ethernet TFTP file transfers



HDMI passthrough + EdkDSP accelerators



- Xilinx Kintex KC705 board
- HD Video pass-through with 30 HD video frame buffers, 1920x1080p60 (0.5s of video)
- Output 1024x768p75
- 6x EdkDSP vector 8xSIMD FP32bit accelerators 175 MHz, peak perf. 16,8 GFLOP
- 6x 8bit PicoBlaze serving as reprogrammable schedulers
- MicroBlaze 32bit 100 MHz
- Xilkernel + LWIP based 1Gb Ethernet Web Server
- 1Gb Ethernet TFTP file transfers

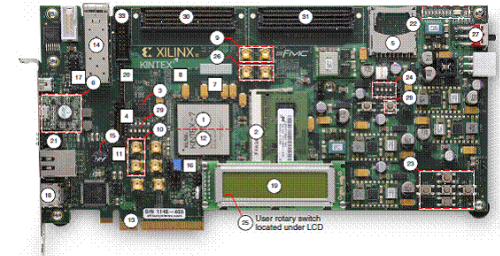


HD Video Processing Chain Demo



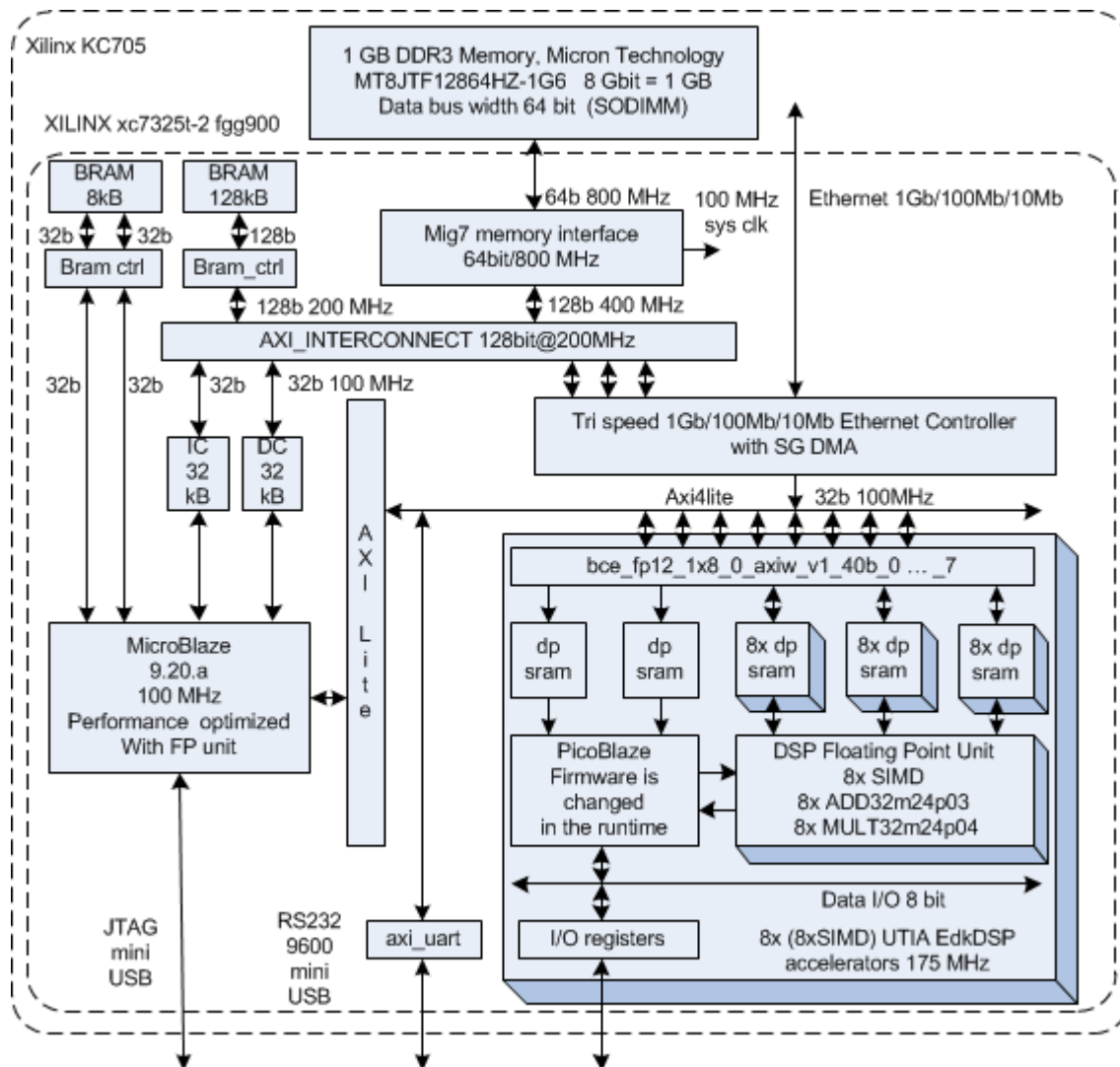
- **Computation and Communication Blocks for Xilinx Kintex7 FPGA with UTIA EdkDSP Accelerators. Vivado 2013.4 Designs with SW Demos.**

- KC705 with 175 MHz EdkDSP accelerators
- EdkDSP accelerators for processing data
- 100 MHz 32bit MicroBlaze CPU,
- 1G Ethernet controller, DDR3 800 MHz
- Xilkernel and LwIP based Web server for status & control
- EdkDSP FP32 accelerators 8x (8xSIMD) 175 MHz
- PicoBlaze6 based schedulers 175 MHz with UTIA C compiler



- http://sp.utia.cz/index.php?ids=results&id=Utia_EdkDSP_Vivado_2013_4_KC705
- Detailed application note (61 pages):
http://sp.utia.cz/results/Utia_EdkDSP_Vivado_2013_4_KC705/Utia_EdkDSP_Vivado_2013_4_KC705.pdf

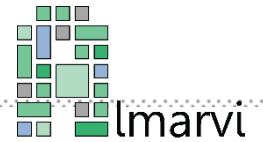
Evaluation package - EdkDSP Accelerators



- **Peak performance (8x 8xSIMD) 22,4 GFLOP/s**
- **Demonstration of performance of a single EdkDSP accelerator:**
- **FIR (1x 8xSIMD) 1,4 GFLOP/s**
- **LMS (1x 8xSIMD) 1,0 GFLOP/s**



Summary of Demonstrated Technology



- **ON Semi CMOS Color Image Sensor
2.3 Megapixel.**
- **HDMI In & Out for Video data**
- **Full HD support (1920x1080p60)**
- **1Gbit Ethernet for configuration, control and GUI**
- **Future work on HW portability (FMC standard):**
 - **ZC702 – 1x HDMI out + 2x FMC Imageon card**
 - **KC705 – 1x HDMI out, 2x FMC Imageon card**
 - **Industrial FMC carriers with ZYNQ System-On-Module**

**This work has been partially supported by the Artemis JU project
ALMARVI No. JU 621439 and Czech MEYS project 7H14004.**