Application Note

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Ústav teorie informace a automatizace AV ČR, v.v.i.

Interfacing e•MMC 32 GB Memory MTFC32GJWDQ-4M with Xilinx ZC702 FPGA Board

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Revision

Revision	Date	Author	Description
0	04.11.2014	Kohout	Initial version

Contents

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1 Description

This application note describes an interfacing e•MMC32 GB non-volatile memory MTFC32GJWDQ-4M with Xilinx ZC702 FPGA board [5] (ZYNQ with dual core ARM Cortex A9). The dual core ARM Cortex A9 inside of the ZYNQ part includes 2 SD/e•MMC interface cores (SDIO). First core is used for SD card to download bitstream into the FPGA and initiate boot sequence. The second core is not used by default configuration, hence its interface can be used to connect external e•MMC memory. The ARM Cortex A9 based ZYNQ processing system SDIO has these parameters [6]:

- The controller is compatible with the standard SD Host Controller Specification Version 2.0 as defined in the SD2.0/SDIO 2.0 specification standards. It supports:
  - SDMA (single operation DMA),
  - ADMA1 (4 KB boundary limited DMA),
  - ADMA2 (ADMA2 allows data of any location and any size to be transferred in a 32-bit system memory with scatter-gather DMA) support.
- The controller core also supports up to seven functions in SD1, SD4, but does not support SPI mode.
- SD High-Speed (SDHS) card standard support.
- SD High Capacity (SDHC) card standard support.
- MMC 3.31 standard support.

The e•MMC flash memories are not primary boot devices for Zynq-7000 family, but can be used as secondary boot devices with connection wired inside of the ZYNQ FPGA fabric. As MTFC32GJWDQ-4M flash memory pupports MMC 4.51 standard, this approach is limited to 4-bit data path and it cannot be extended to the complete 8-bit transfer mode.

2 Implementation

To implement pass-trough logic between second SDIO controller of the ZYNQ and externally located flash memory was used Xilinx Vivado 2013.4 tool. The block diagram of it is shown in Figure 1.

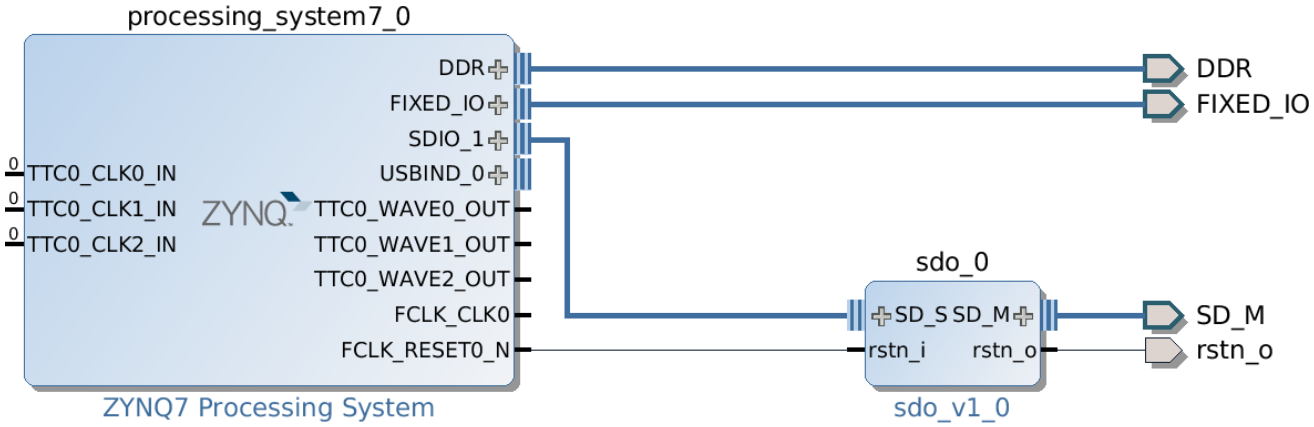

Figure 1: Interface of the second ZYNQ SDIO controller implemented in the ZYNQ FPGA fabric for 4-bit to the e•MMC memory on ZC702 board.

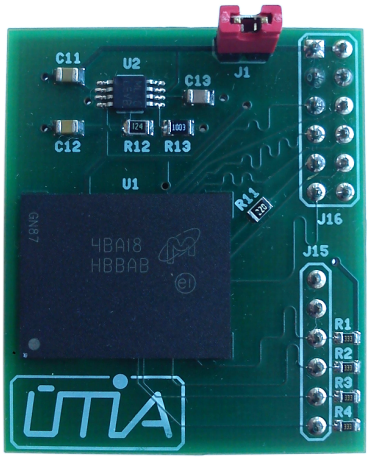

Figure 2: e•MMC 32 GB Memory MTFC32GJWDQ-4M Board.

2.1 Required HW

The list below summarizes HW components needed to access e•MMC memory from ZC702 board:

- ZC702 Evaluation Board for the Zynq-7000 XC7Z020 [5]. This board provides SD/e•MMC controller.
- FMC XM105 Debug Card [4] to expand ZC702 FMC connector.
- e•MMC 32 GB Memory MTFC32GJWDQ-4M Board (see Figure 2). To get detailed information about the board contact ÚTIA, Department of Signal Processing on this e-mail: matulik@utia.cas.cz.

Altogether connected HW components are shown in Figure 3.

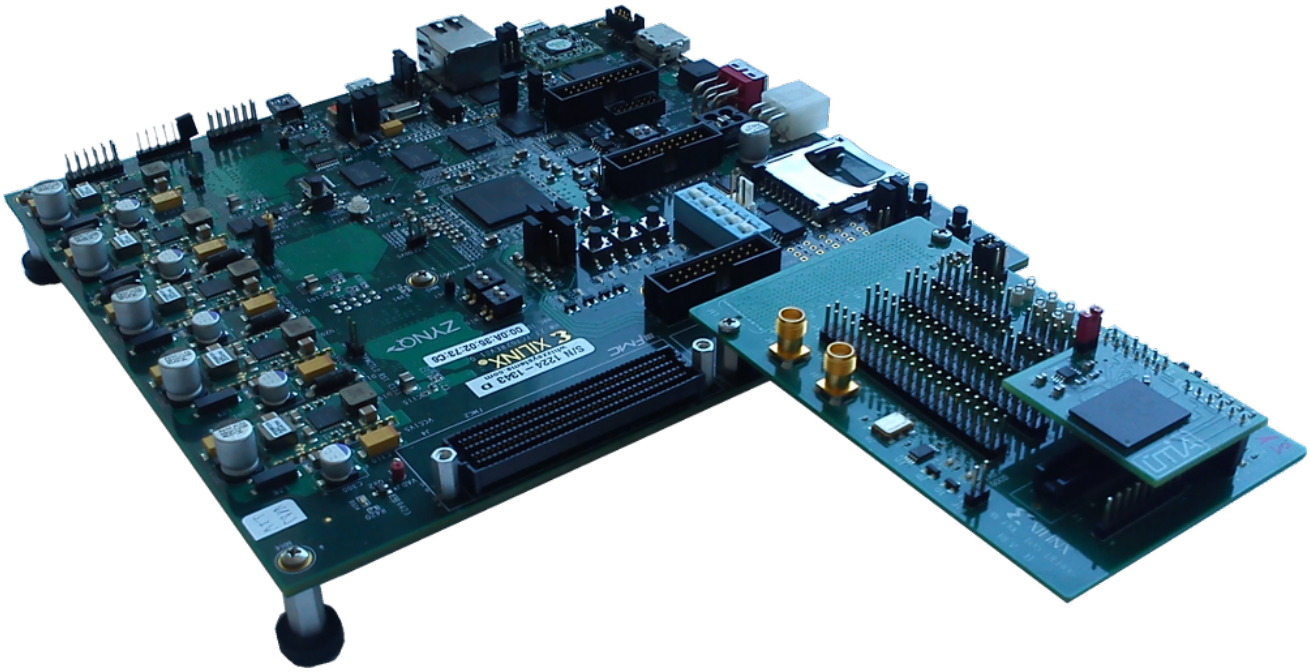

Figure 3: Set of ZC702, XM105 and e•MMC32 GB Memory MTFC32GJWDQ-4M Boards.

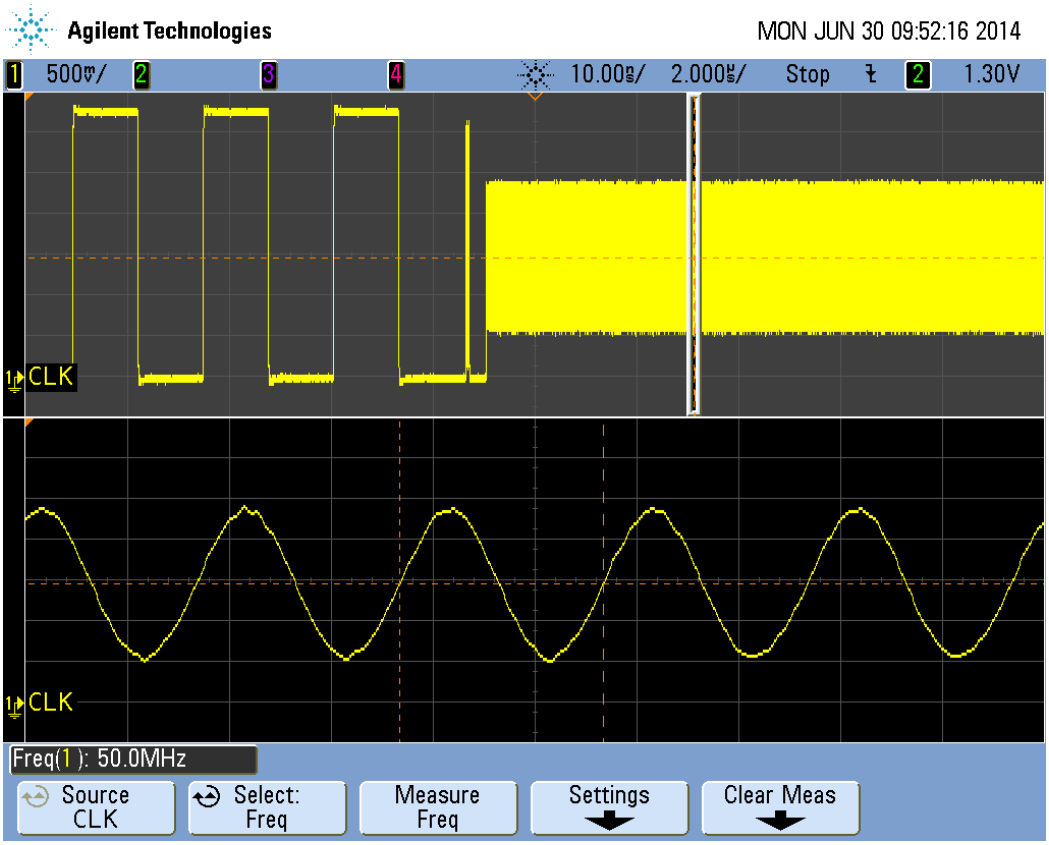

Figure 4: Oscilloscope snapshot - Clock Speed Change.

3 Initial Setup

Initial setup consists of steps enumerated below:

1. Initailze second SDIO controller to be a MMC host.
2. Read OCR, CID and CSD registers from the e•MMCmemory.
3. Set bus to 4-bit mode.
4. Set bus speed to 50 MHz. The clock speed change is depicted in Figure 4.
5. Read EXT_CSD register.

Until the bus speed is switched to 50 MHz, the communication runs at slow mode using 380 kHz clock. Reading OCR, CID and CSD registers uses solely command line, but the reading EXT_CSD register uses all of 4 data lines to obtain its content.

The structure of OCR, CID and CSD registers is listed in text below. Information decoded from these registers corresponds to structure presented in MMC System Specification version 3.31 [1]. As the MMC standard in version 3.31 does not specify EXT_SCD register, its value is listed without the structure description. It should be noted that the OCR, CID and CSD structure could be slightly different compare to MMC 4.51 standard.

3.1 Operation Condition register OCR

Value:

```
C0FF8080

Power ON status:        1
2.7-3.6V:               0x1FF
2.0-2.6V:               0x00
1.65-1.95V:             1
```

3.2 CardID register CID

Value:

```
0x00FE014E 4D4D4333 32471088 4458EA11

MID:                    0xFE
OID:                    0x014E
PNM:                    MMC32G
PRV:                    1.0
PSN:                    2554616042
MTD:                    2014, January
```

3.3 Card Specific Data register CSD

Value:

```
00D06E01 320F5913 FFFFFFFF FF924000

CSD_STRUCTURE:          Reserved
SPEC_VERS:              Reserved
TAAC:                   Time unit - 1 ms, Mult factor - 6.0
NSAC:                   1 * 100 CC
TRAN_SPEED:             Freq unit - 10 Mb/s, Mult factor - 2.5
CCC:                    Supported command classes - 0 2 4 5 6 7
READ_BL_LEN:            512 B
READ_BL_PARTIAL:        0
WRITE_BLK_MISALIGN:     0
READ_BLK_MISALIGN:      0
DSR_IMP:                1
C_SIZE:                 4095
VDD_R_CURR_MIN:         100 mA
VDD_R_CURR_MAX:         200 mA
VDD_W_CURR_MIN:         100 mA
VDD_W_CURR_MAX:         200 mA
C_SIZE_MULT:            512
ERASE_GRP_SIZE:         31
ERASE_GRP_MULT:         31
WP_GRP_SIZE:            32 GB
WP_GRP_ENABLE:          1
DEFAULT_ECC:            0
```

```
R2W_FACTOR:             16
WRITE_BL_LEN:           512 B
WRITE_BL_PARTIAL:       0
CONTENT_PROT_APP:       0
FILE_FORMAT_GRP:        0
COPY:                   0
PERM_WRITE_PROTECT:     0
FILE_FORMAT:            HDD-like FS with partition adma_table
ECC:                    None (default)
```

3.4 Extended Card Specific Data register ECSD

Value (bytes 511 downto 0):

```
00 00 00 00 00 00 00 01 03 01 3F 3F 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
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00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 19 FF 00 00 00 00 00 32 00
04 09 09 00 00 00 00 0F 55 06 09 07 00 80 07 10
01 01 04 06 09 00 10 00 03 A2 00 00 00 08 08 08
08 08 08 00 02 02 05 05 01 04 0F 17 00 02 00 06
00 00 00 00 00 00 01 00 01 00 00 00 00 00 00 00
00 00 00 00 00 00 00 01 1F 05 00 00 00 00 00 03
00 01 D1 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 01 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
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```

4 Performance

Details of performance measurement setup:

- Evaluation board ZC702 with ZYNQ xc7z020-1.
- ARM processor clock 666 MHz.
- DDR3 (32 bit data bus) 533 MHz.
- ARM SDIO controllers used:
  - SDIO_0 to access SD card reader of ZC702 board.
  - SDIO_1 connected via the FPGA fabric of ZYNQ xc7z020-1 ES part (see Figure 1) via the FMC1 connector to FMC XM105 Debug board and via the PCB to the e•MMC memory MTFC32GJWDQ-4M.
  - SIDO_1 initial clock speed 380 kHz and open collector communication.
  - SIDO_1 normal mode for data WR and data RD at clock speed 50 MHz.
  - 4-bit data bus. This is given by the limitation of the ARM Cortex A9 dual core processor SDIO_0 and SDIO_1 controller to 1 bit or 4 bit communication.
  - Single data rate. This is also given by the limitation of the ARM Cortex A9 dual core processor SDIO_0 and SDIO_1 controller present in ZYNQ.
- The FPGA I/O bank standard is 3.3 V.
- The power supply for the 32 GB e•MMC part MTFC32GJWDQ-4M has been set to 2,75 V. This is just above the minimum voltage specification 2,7 V.
- SW part of the evaluation setup performs:
  - Initial setup using slow clock 380 kHz and switch to 50 MHz clock.
  - Write of 1 MB randomly generated data in 512 Byte blocks, without ADMA.
  - Readback of 1 MB of data in 512 Byte blocks, without ADMA.
  - Verification of 1 MB data after read. It is not part of the time measurement.

Figure 5 shows plot related to measurement of time needed to write 1 MB block of data to e•MMC. The time is 47.1746 ms that implies the reached performance is 21.198 MB/s. Figure 5 indicates one interval, where the process of writing to the memory was temporarily stopped by the communication interface. This is due to the fact that the written memory is busy (see DATA0 line in Figure 5). The measurement of the write operation takes this delay in to account.

Figure 6 shows plot related to measurement of time needed to read 1 MB block of data from e•MMC memory. The time is 43.88 ms which means that the performance is 22.79 MB/s.

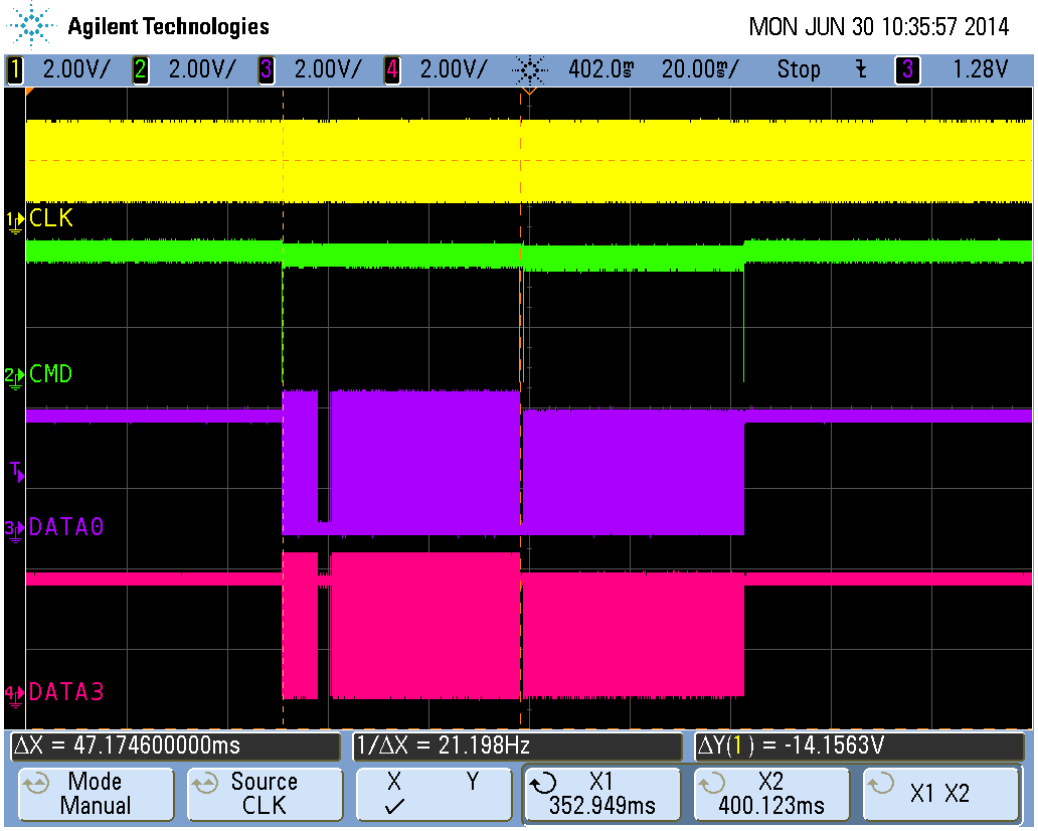

Figure 5: Oscilloscope snapshot - Measured performance 1 MB WR to e•MMC is 21.198 MB/s.

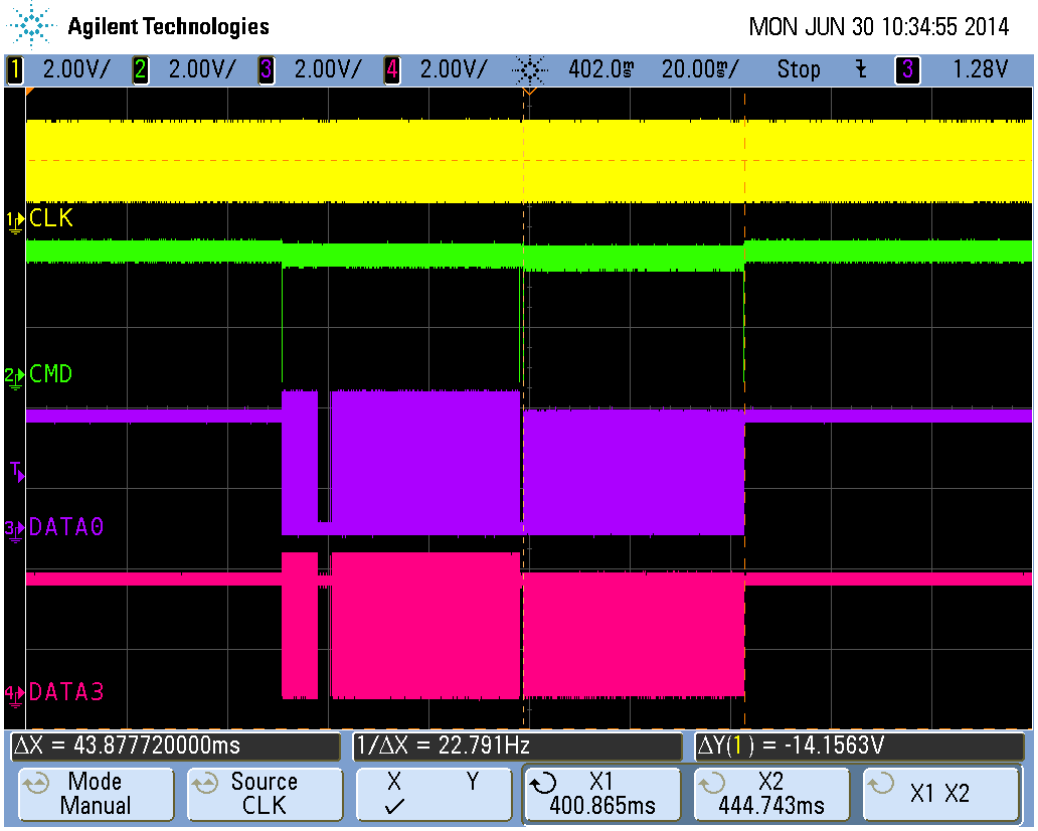

Figure 6: Oscilloscope snapshot - Measured performance for 1 MB RD from e•MMC is 22.791 MB/s.

5 Quickstart

1. Configure ZC702 VADJ voltage to 3.3 V, use USB Interface Adapter EVM [3] (see HOWTO [2]).
2. Plug XM105 Debug card into FMC1 connector on ZC702 board.
3. Install a shunt on connector J6.1 to J6.3 and another shunt on connector J6.2 to J6.4 to connect the board 3.3 V power to the HDR_POWER net on connector J16.1 and J16.2 on XM105 Debug card.
4. Install a shunt on connector J5.6 to J5.7 of XM105 Debug card to close JTAG chain.
5. Disconnect LEDs DS1, DS2, DS3 and DS4 on XM105 Debug card (remove these LEDs or related rezistors R1, R2, R3 and R4).
6. Plug e•MMC 32 GB Memory MTFC32GJWDQ-4M board into the XM105 Debug card, related connectors are J15 and J16.
7. Copy ZC702 boot image *boot.bin* (see section 6) on SD card, insert the card to the ZC702 SD card reader.
8. Set ZC702 board to boot from the SD card. Set switch SW16 to value 0b00110.
9. Plug the USB UART cable in. Serial terminal settings are:
   - Baudrate: 115200
   - Data bits: 8
   - Stop bits: 1
   - No parity
   - No control flow
10. Switch ZC702 board power on.
11. Observe the software terminal.
12. Control the application by the terminal, Table 1 presents application controls.

Table 1: Application controls.

Key	Description
s	Prepare random data to write
w	Write
r	Read and compare
W	Print write buffer
R	Print Read buffer
m	Print this menu
x	Quit

6 Package Content

```
.
|-- doc
|   \-- appnote
\-- bin
    \-- boot.bin
```

References

[1] MMCA Technical Committee. The MultiMediaCard - System Specification Version 3.31. http://read.pudn.com/downloads92/ebook/361855/MMC-System-Spec-v3.31-free.pdf, 2003.

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[3] TI. USB Interface Adapter EVM. http://www.ti.com/tool/usb-to-gpio.

[4] Xilinx. FMC XM105 Debug Card User Guide UG537 (v1.3). http://www.xilinx.com/support/documentation/boards_and_kits/ug537.pdf, 2011.

[5] Xilinx. ZC702 Evaluation Board for the Zynq-7000 XC7Z020 All Programmable SoC User Guide UG850 (v1.2). http://www.xilinx.com/support/documentation/boards_and_kits/zc702_zvik/ug850-zc702-eval-bd.pdf, 2013.

[6] Xilinx. Zynq-7000 All Programmable SoC Technical Reference Manual UG585 (v1.8.1). http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf, 2014.