Application Note

Akademie věd České republiky
Ústav teorie informace a automatizace AV ČR, v.v.i.

Dynamic PL reconfiguration for Zynq

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Contents

Revision history

Rev.	Date	Author	Description
1	18.12.2014	Z.P.	Initial version
2			
3			

1. Introduction

The architecture of the Zynq all programmable SoC from Xilinx consists of Dual ARM Cortex-A9 cores with NEON DSP/FPU engine and of programmable logic (PL). This demo shows how the PL can be fully reconfigured without using partial dynamic reconfiguration. This way, at the cost of the longer time needed for reconfiguration of PL we can cover 90% typical applications using dynamic reconfiguration where CPU cores are running while PL adapts.

2. Description

The design consists of three parts – Vivado projects for first and second PL bitstream and SDK workspace. In the SDK workspace, the application demonstrating the PL reconfiguration, reset and clock settings for PL can be found. The precompiled content of the SD card and necessary bitstreams for PL configuration for ZC702 evaluation board can be found in boot_image/sd_card

The demo version of the package contains bitstreams and software in form of pre-compiled binaries.

2.1 FPGA

The PL design contains simple counter. Two configurations differs only in direction of counting. Block design of the PL can be found in the Figure 1.

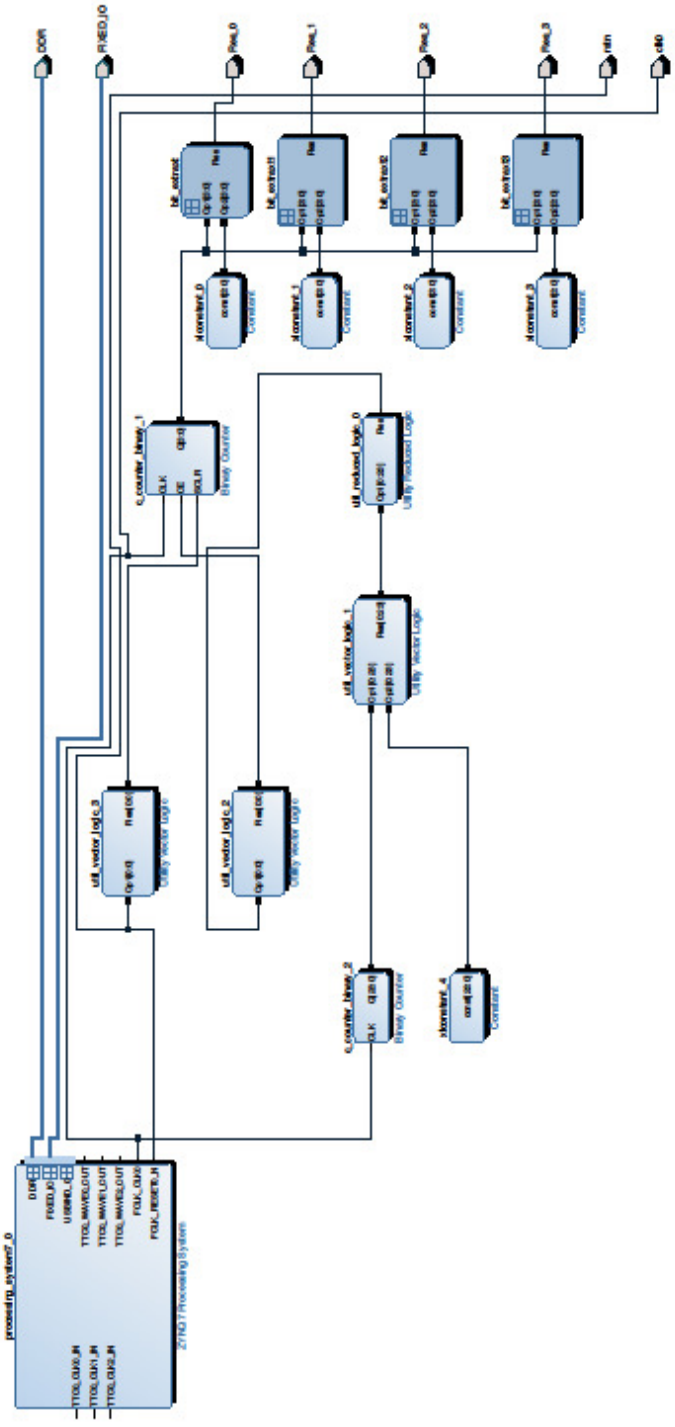

Figure 1: Block design for PL in ZC7020

3. Used tools and resources

Xilinx Vivado 2013.4, SDK. SDHC card reader..

4. Implementation

1. Demo package users please skip directly to step 9.
2. Compile pl_design1
   a. Open Vivado project pl_design1

   b. Check –bin_file at bitstream settings window
   c. Compile to bistreams
3. Compile pl_desing2
   a. In the same way as pl_design1
4. Open pl_design1 or 2
   a. Export hw to SDK and start SDK.
5. Create fsbl project from template together with fsbl_bsp
6. Create empty application project named pl_reconfig, use the same fsbl_bsp
   a. Copy provided sources to src subdir
7. Compile all software projects
8. Go to boot_image dir and run make.bat in shell command line (lauched from SDK Xilinx Tools menu item)
9. Copy all contents of sd_card subdirectory to SD card root.
10. Switch SW16 on ZC702 to 0,0,1,1,0 (boot from SD).
11. Connect USB UART to PC and run serial terminal : 115200bps, 8bit, 0parity, 1stop
12. Power the ZC702 and use terminal to initiate reconfigurations

```
Devcfg driver initialized
SD: rc= 00000000
Read b1.bin to addr 0x20000000, length 0x3DBAFC bytes
Read b2.bin to addr 0x30000000, length 0x3DBAFC bytes
*********************************
* UTIA AV CR, v.v.i
* FPGA Reconfguration Demo
* 16.12.2014
*********************************

 1 - Set all FCLK_RESETx_N (active low)
 2 - Reset PL fabric, configure bitstream1 (FSBL PCAP)
 3 - Reset PL fabric, configure bitstream2 (FSBL PCAP)
 4 - Release all FCLK_RESETx_N signals
 5 - Set FCLK_CLK0 frequency <1,64>
 6 - Get DIE temperature
 7 - Get silicon version
>
```

Figure 2: Example serial terminal communication

5. Troubleshooting

- To get PL reconfiguration working, the design must be booted from SD card (not via JTAG from SDK). After SD card boot finishes, it is possible to use SDK and JTAG for debugging.
- UART terminal must be connected after the ZC702 board is powered on.

6. Acknowledgements

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7. Package contents

cdrom	- boot_image	precompiled binaries and sd card boot files
	- doc	This documentation
	- pl_design1	project for first PL configuration (count up)
	- pl_design2	project for second PL configuration (count down)
	- Workspace	software project directory, demo version has only pre-compiled binaries here

8. References