

## Introduction

The Utility IO Multiplexer module provides a multiplexing function between two IO vectors to one IO vector.

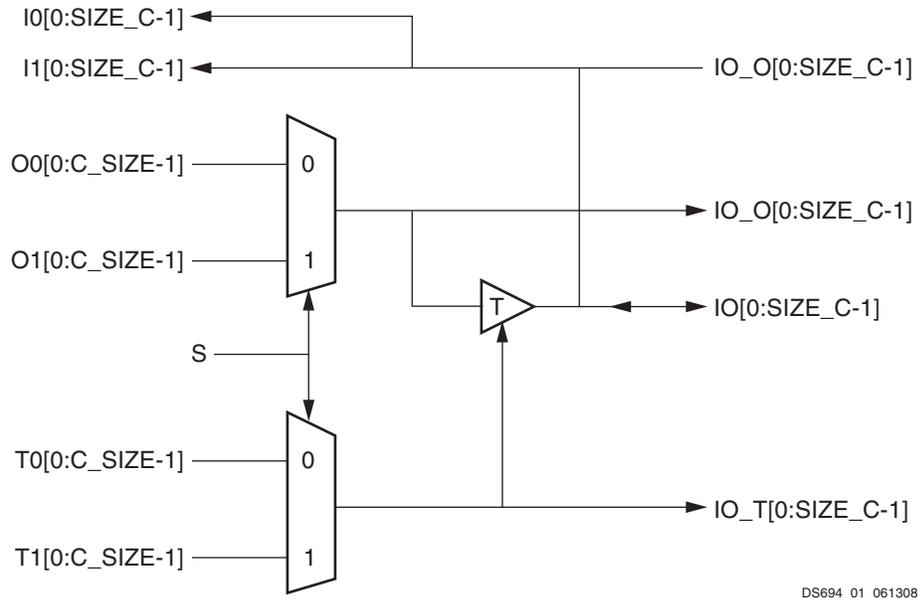
## Features

- Provides 2 to 1 multiplexing of IO vectors
- Configurable size of vectors

LogiCORE™ Facts		
<b>Core Specifics</b>		
Supported Device Family	See <a href="#">EDK Supported Device Families</a> .	
Version of core	v1.00a	
<b>Resources Used</b>		
	Min	Max
LUTs	1	2*C_SIZE
FFs	N/A	N/A
Block RAMs	N/A	N/A
DCMs	N/A	N/A
PLLs	N/A	N/A
<b>Provided with Core</b>		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs & application notes	None	
Additional Items	None	
<b>Design Tool Requirements</b>		
Xilinx Implementation Tools	See <a href="#">Tools</a> for requirements.	
Verification		
Simulation		
Synthesis		
<b>Support</b>		
<a href="#">Xilinx, Inc.</a>		

## Functional Description

The block diagram for the Utility IO Multiplexer module is shown in [Figure 1](#).



*Figure 0: Utility IO Multiplexer Block Diagram*

The Utility IO Multiplexer provides a way of selecting which of two IO vectors should be connected to one IO vector. The size of the vectors is determined by the parameter *C\_SIZE*, which has the minimum value 1.

## Utility IO Multiplexer I/O Signals

The interface signals for the Utility IO Multiplexer module are listed and described in [Table 1](#).

*Table 1: Utility IO Multiplexer Signal Descriptions*

Signal Name	I/O	Initial State	Description
I0	O		Input vector 0 [0:C_SIZE-1]
O0	I		Output vector 0 [0:C_SIZE-1]
T0	I		Tristate disable vector 0 [0:C_SIZE-1]
I1	O		Input vector 1 [0:C_SIZE-1]
O1	I		Output vector 1 [0:C_SIZE-1]
T1	I		Tristate disable vector 1 [0:C_SIZE-1]
S	I		Input select signal. 0 : O0 and T0 drives, IO_O and IO_T respectively 1 : O1 and T1 drives, IO_O and IO_T respectively

**Table 1: Utility IO Multiplexer Signal Descriptions (Cont'd)**

Signal Name	I/O	Initial State	Description
IO_I	I		IO input vector [0:C_SIZE-1]
IO_O	O		IO output vector [0:C_SIZE-1]
IO_T	O		IO tristate disable vector [0:C_SIZE-1]
IO	IO		IO tristate vector [0:C_SIZE-1]

## Design Parameters

The parameters defined for the Utility IO Multiplexer module are listed and described in [Table 2](#).

**Table 2: Utility IO Multiplexer Parameters**

Parameter Name	Feature Description	Allowable Values	Default	VHDL Type
C_SIZE	The size of the vectors	natural	8	integer

## Parameter - Port Dependencies

The affects of setting various parameters is shown in [Table 3](#).

**Table 3: Utility IO Multiplexer Parameter-Port Dependencies**

Parameter	Port	Description
C_SIZE	IO, O0, T0, I1, O1, T1, IO_I, IO_O, IO_T, IO	Size of vectors

## Design Implementation

### Target Technology

The target technology is an FPGA listed in [EDK Supported Device Families](#).

### Device Utilization and Performance Benchmarks

The device utilization depends on the size of the vectors being multiplexed.

### Specification Exceptions

Not Applicable.

### Reference Documents

None

## Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

## Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
6/13/08	1.0	Initial Xilinx release.
4/24/09	1.1	Replaced references to supported device families, tool name(s), and parameter values with hyperlink to PDF file; converted to current DS template.

## Notice of Disclaimer

Xilinx is providing this product documentation, hereinafter "Information," to you "AS IS" with no warranty of any kind, express or implied. Xilinx makes no representation that the Information, or any particular implementation thereof, is free from any claims of infringement. You are responsible for obtaining any rights you may require for any implementation based on the Information. All specifications are subject to change without notice. XILINX EXPRESSLY DISCLAIMS ANY WARRANTY WHATSOEVER WITH RESPECT TO THE ADEQUACY OF THE INFORMATION OR ANY IMPLEMENTATION BASED THEREON, INCLUDING BUT NOT LIMITED TO ANY WARRANTIES OR REPRESENTATIONS THAT THIS IMPLEMENTATION IS FREE FROM CLAIMS OF INFRINGEMENT AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Except as stated herein, none of the Information may be copied, reproduced, distributed, republished, downloaded, displayed, posted, or transmitted in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx.