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Reconfigurable Image Processing Accelerator

Project Goals

To prepare

- mixed FPGA/DSP architecture for
  - High speed raster processing
  - Low-power raster processing
  - Embedded raster processing (intelligent cameras, etc.)
- Configuration support for this system (simple and flexible configuration scripts)
- Prototyping support (easy-to-use front-end with export to scripts)

Motivation

- DSP: high speed, simple design
- FPGA: possibly massively parallel, hence very efficient for image manipulations
- Both DSP and FPGA: relatively low energy consumption (embedded devices)

BUT

- complex technology & design tools

Acceleration Platform

TI TMS320C6416 + Xilinx Virtex II – 250

Expected Benefits

- Integration of Simulink prototyping
- Support for easy in-situ scripting
- Rapid prototyping support
- SW and HW algorithm libraries

Project Status

- Project duration 2004-2008
- Design of system architecture
- Evaluation of scripting systém
- Simulation of functional units
- Communication systems ready

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